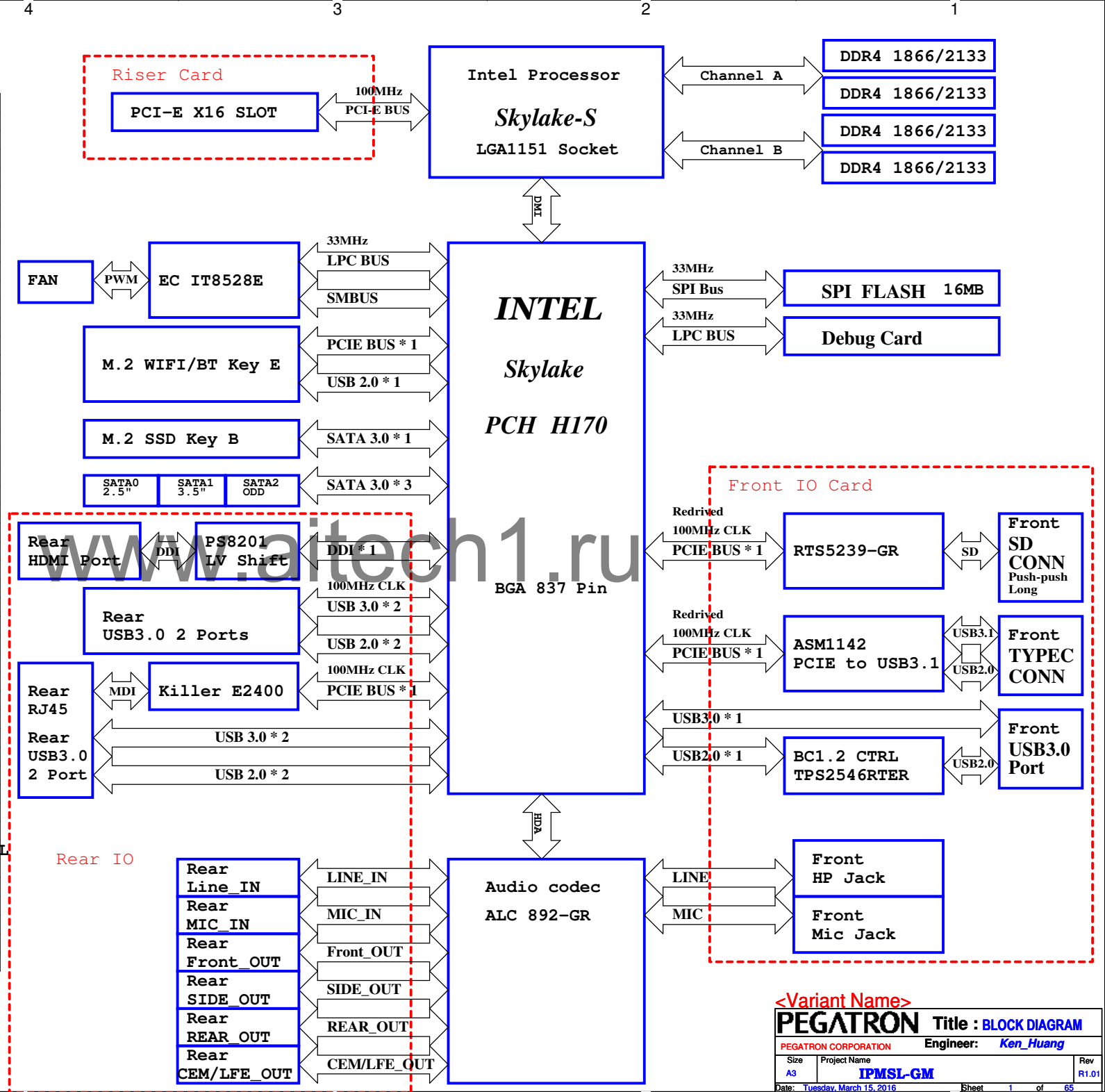


# IPMSL-GM

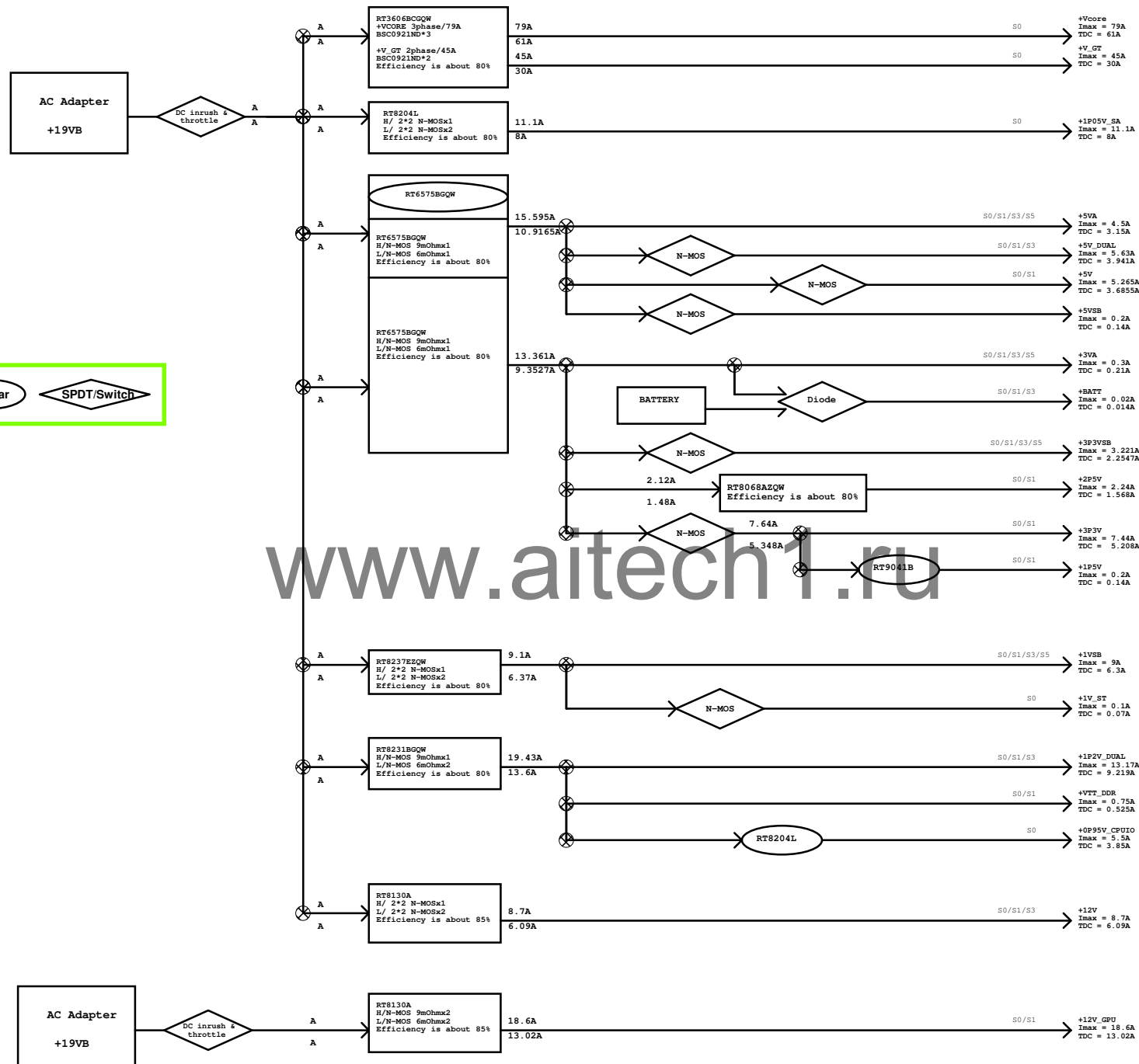
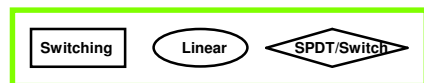
Revision: 1.00

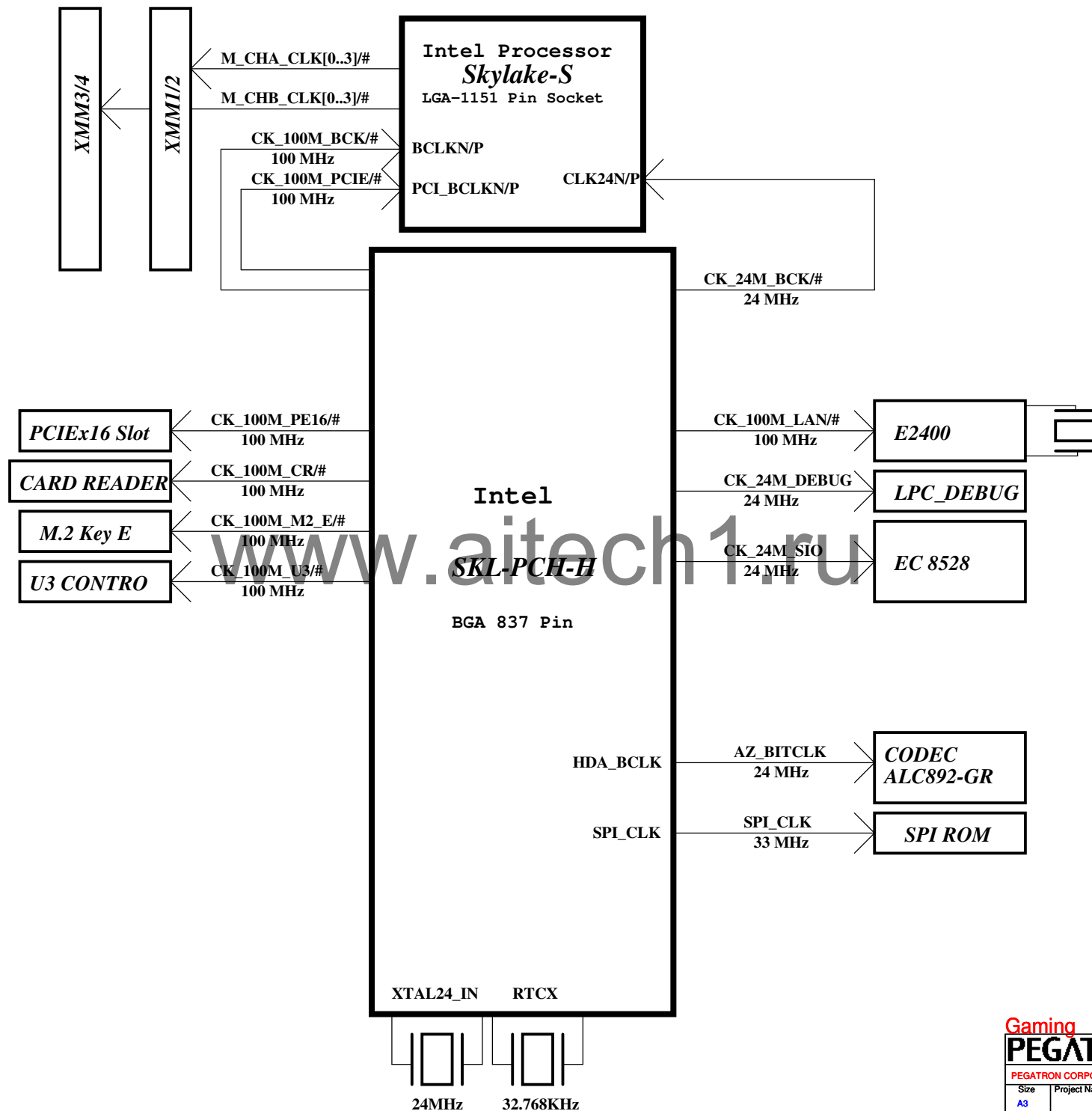
PAGE	TITLE
01	BLOCK DIAGRAM
02	CHANGE HISTORY
03	Power FLOW
04	Clock Distribution
05	Power Sequence
06	POWER DISTRIBUTION
07~12	CPU
13~16	DDR4
17	DDR4 TERMINATION A&B
18~25	PCH
26	PCH_PLTRST
27	EC IT8528E
28	M2 WIFI REDRIVER
29	M.2 WIFI/BT KEY A
30	M.2 SSD REDRIVER
31	M.2 SSD KEY M
32	PCIE X16 SLOT
33	AUDIO CODEC ALC892-CG
34	AUDIO REAR CONNECTOR
35	LAN E2400
36	RJ45 + USB3.0
37	REAR USB3.0
38	HDMI REPEATER
39	HDMI CONNECTOR
40	Front Panel
41	SATA CONNECTOR + SATA POWER CONN
42	CPU / SYS FAN
43	Power Button / LED
44	Debug LED
45	LED Lighting Bar
46	SMBUS/SPI
47	RTC/CMOS
48	LPC DEBUG
49	+19VSB SYSTEM
50~55	Vcore & VCCGT
55	+1P05V_SA & +0P95V_CPUIO
56	+1.2V_DUAL
57	+2P5V_VPP
58	+1VSB
59	+3P3V +5V +1V_ST +3P3VSB +5V_DUAL
60	+12V SYSTEM
61	+5VSB +3VA +5VA
62	+1P5V
63	+19VSB GPU
64	+12V_GPU
65	POWER DISCHARGE



## Schematics Change History

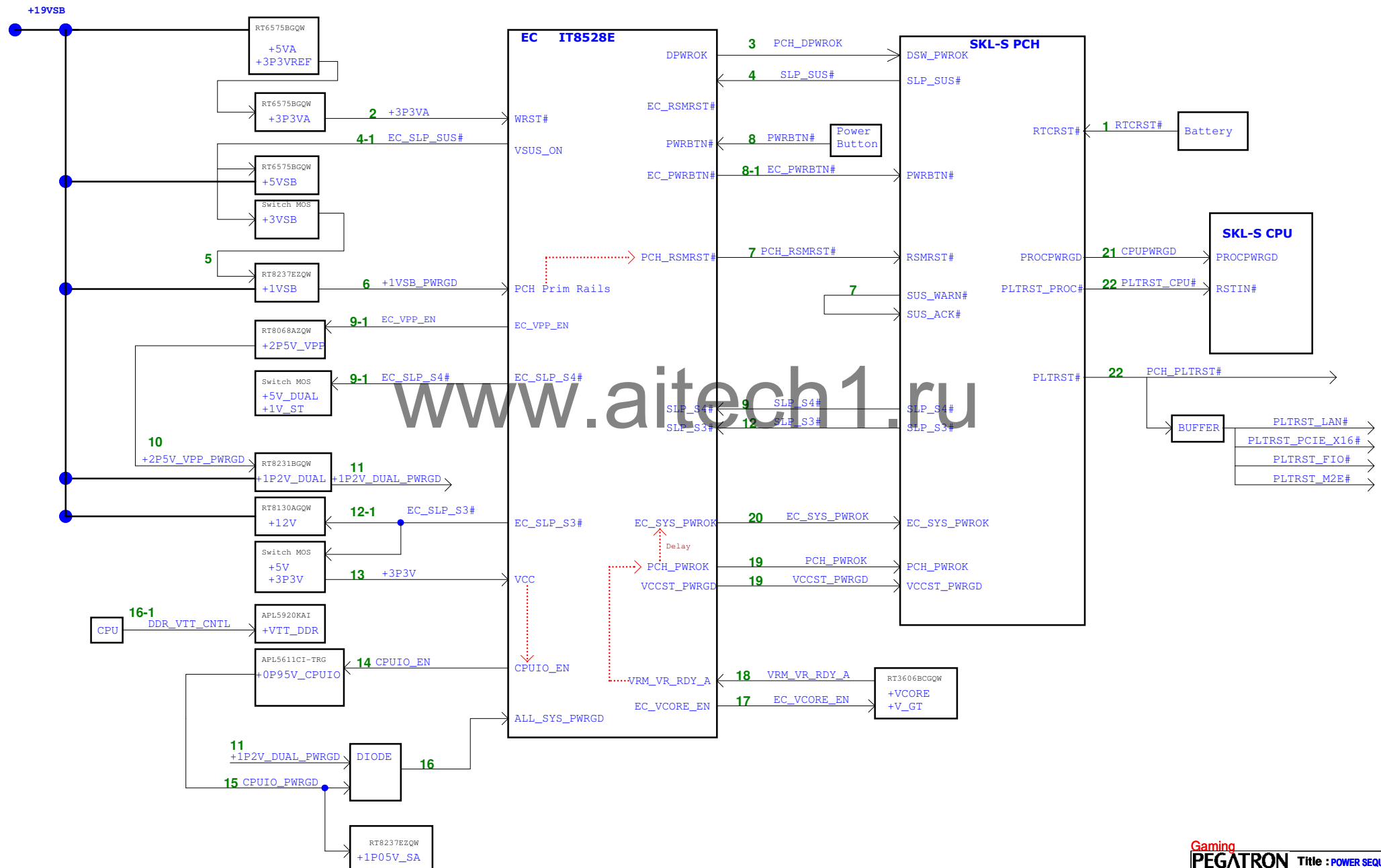
Version	Change list	Version	Change list	Version	Change list
1.00	First release		Add RSMRST discharge circuit		
1.01	P.57 Power circuit net name		Add DPWROK discharge circuit		
	PCIE Port9 ~ Port12 for M2 SSD	1.02	P77 change to 1217-000E000		
	DEVSLP Move to GPP_E4 (SATA Port mapping)		PR187 change to 10X220750000 for +5VA		
	Change Lan connector		Discharge circuit (3P3VSB change to 3VA)		
	Audio : Centor and Rear exchanged		Add MOS to ID of 8 PIN Connector		
	3PIN Fan change to 4PIN Fan		Board ID change to 01		
	Card Reader resistor (PD/PU)		19V LED change to I		
	BIOS ROM change to 16MB		CR9 change to BLUE LED		
	E69 change to 1x3 (Remove password)		CON17 change to 1215-01KB000		
	Thermistor change to PD		XMM3, XMM4 change to RED SLOT		
	LC71, LC72 change to 12PF for 25 MHz crystal		XMM1, XMM2 change to 1202-016F000 (EAR)		
	Add E14 for Acer spec		PR595 change to 21K (for OCP)		
	PC268, PC269 delete (+12V)		Page50 modify 7resistors (Vcore)		
	XCE14 Delete		Change PL52 to 3.3 uH (For system 12V)		
	PQ3 change to PQ136, PQ137		Change P79 to Black color		
	PQ125 change to PQ138, PQ139				
	AQ20 change to PNP BJT for mute signal		Change P71 to Black color		
	Add +12V Discharge		Change CON18 part and symbol (18 PIN)		
	Add UFP Detect signal		Remove PR626		
	SATA Connector change to RED		ADD PC614 PC615 for +5V_AUX		
	Change sys fan connector	1.03	PR67, PR69, PR68,PR70,PR80,PR81,PR83,PR84 for Vore		
	Delete 3 PIN fan circuit		Change PL52 to big size		
	Add WIFI Redriver		Change AR330, AR331 to 1K for Mute		
	Add SSD Redriver		Add AR344 for Mute		
	Support Deep Mode Charging		ECR92, ECR93 NI for LED Bar		
	Change FPC connector		Add +3P3V_DUAL for LED BAR		
	Change XMM4, XMM2 to RED				
	Change ECR73~77 to 33 OHM for EA		SR801,SR802,ECR94,LR34,R55~R59 (short pin)		







### Power On Sequence Diagram G3-S5-S0 (Non Deep)



	<b>CPU Skylake-S 42</b>
+VCORE	-> 79A (Imax) - 65W
+0P95V_CPUIO	-> 5.5A (Imax) - 5.225W
+1P05V_SA	-> 11.1A (Imax) - 11.655W

	<b>PCH</b>
+1VSB	->9A - 9W
+3P3V	-> 0.1A -0.33 W
+3P3VSB	-> 0.8A - 2.64W
+3P3VA	-> 0.2A - 0.66W
+BATT	RTC(G3) ->0.01A - 0.033W

	<b>DDR4 DIMM (4) &amp; Termination</b>
+1P2V_DAU1	-> 10.37 A - 12.44W
+VPP (2.5V)	-> 2.24 A - 5.6 W
+VTT_DDR(0.75V)	-> 0.75A - 0.56W

	<b>PCI Express x 16</b>
+12V	-> 5.5A - 66W
+3P3V	->2A - 6.6W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	<b>LAN E2400</b>
+3P3VSB	->0.5A -1.65W

	<b>EC IT8528E</b>
+3P3VA	-> 0.1A - 0.33W

	<b>ALC892-CG</b>
+3P3VSB	-> 0.05A -0.165W

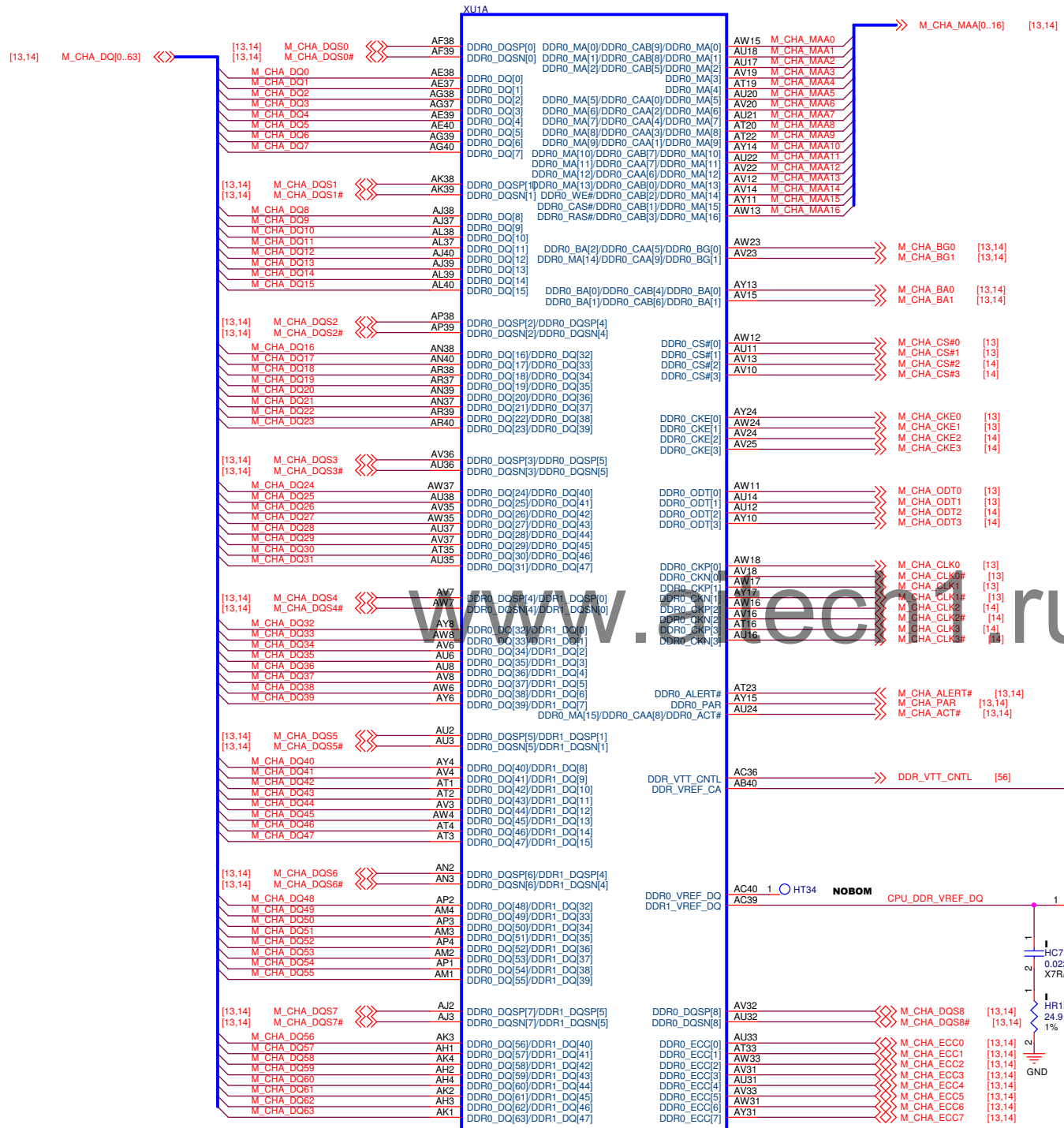
+5V_DUAL	<b>USB3.0 5 PORTS</b>
	(S0, S1) ->5.1A - 25.5W

+3P3VSB	<b>M.2 Key E</b>
	-> 1A -3.3 W

+5V	<b>HDMI</b>
+3P3V	-> 0.5A - 2.5W
+3P3V	-> 1A - 3.3W

+3P3V	<b>M.2 Key B</b>
	-> 2A -6.6 W

+12V	<b>FANS</b>
	-> 1.2A - 14.4W



**NOTE:**  
DDR\_VTT\_CNTL; Disables the platform memory VTT regulator in C8 and deeper and S3.

Gaming

PEGATRON

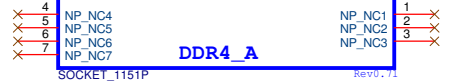
Title : CPU\_DDR4\_A

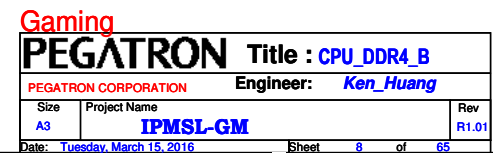
PEGATRON CORPORATION

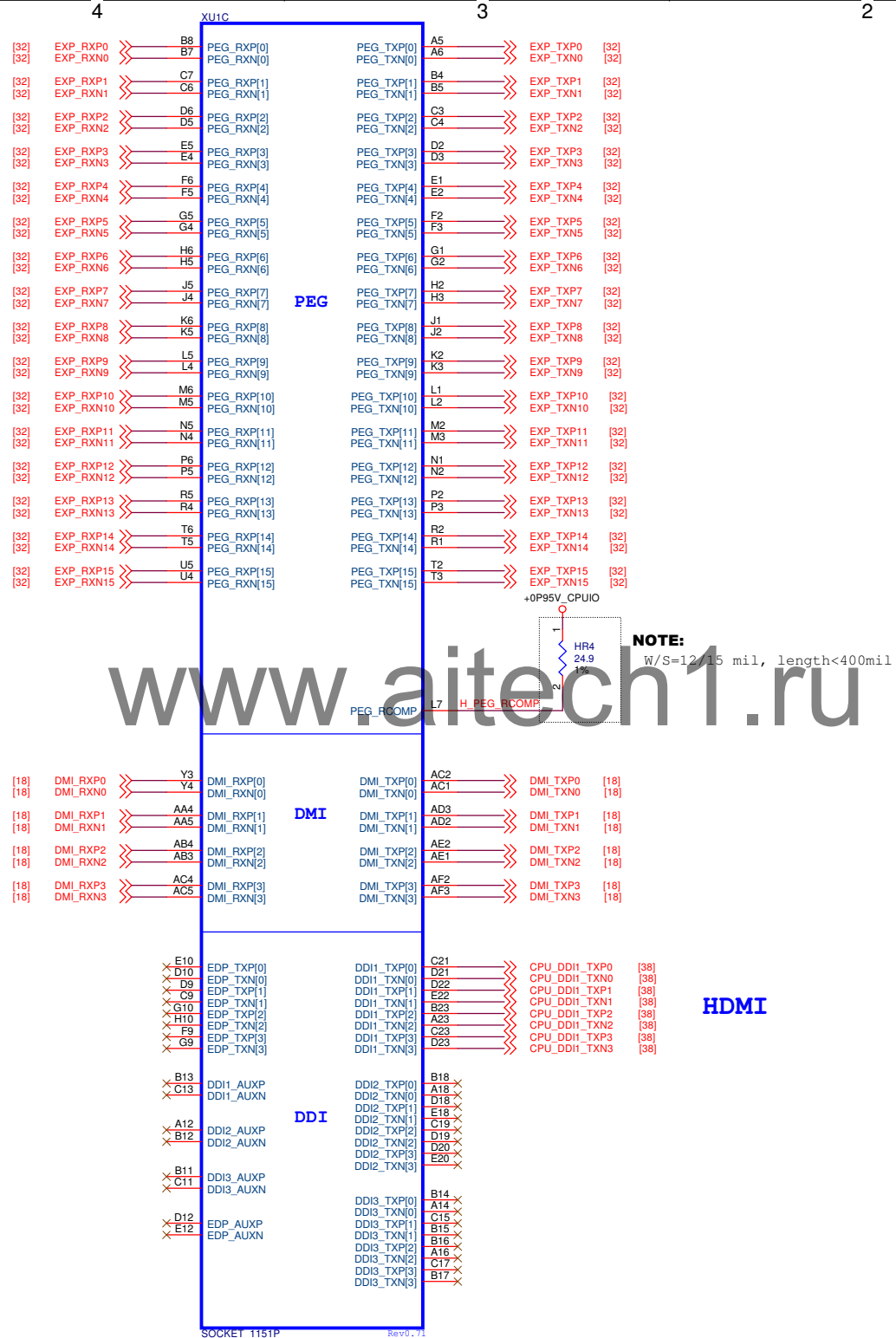
Engineer: Ken\_Huang

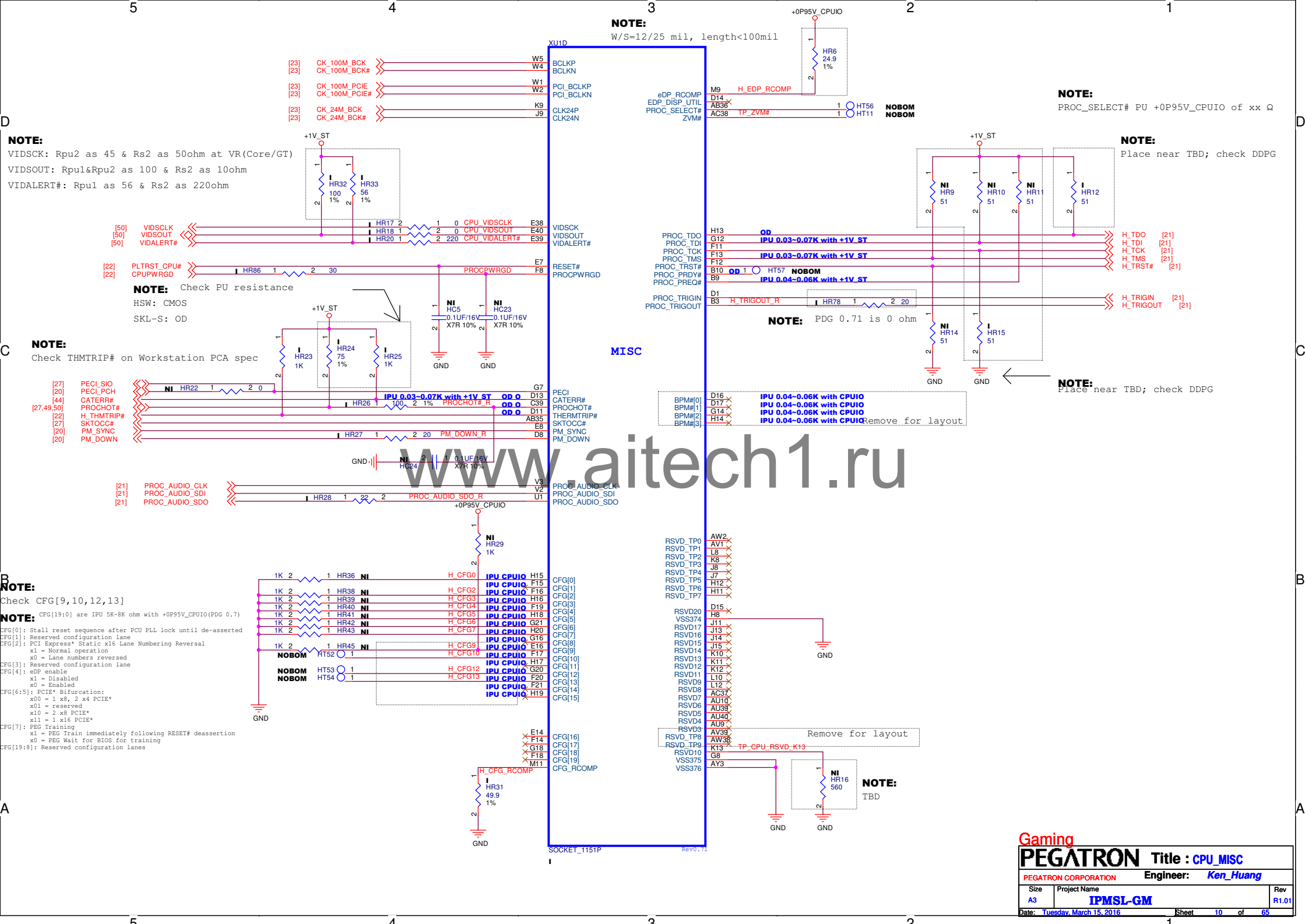
Size	Project Name	Rev
A3	IPMSL-GM	R1.01

Date: Tuesday, March 15, 2016Sheet 7 of 65



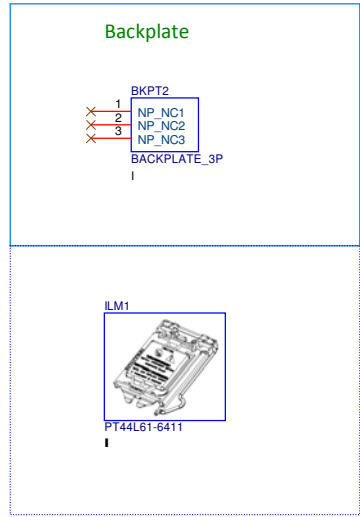
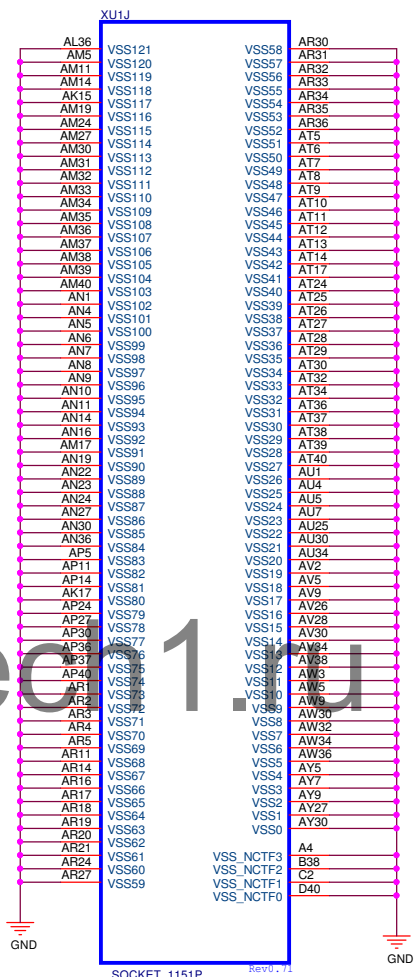
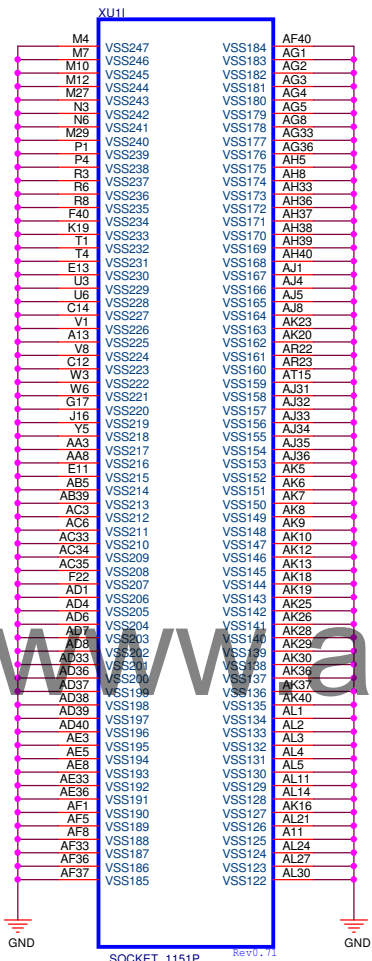
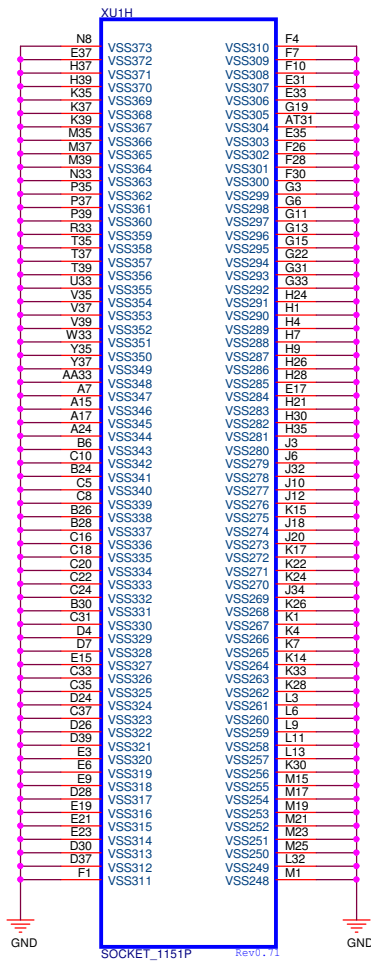






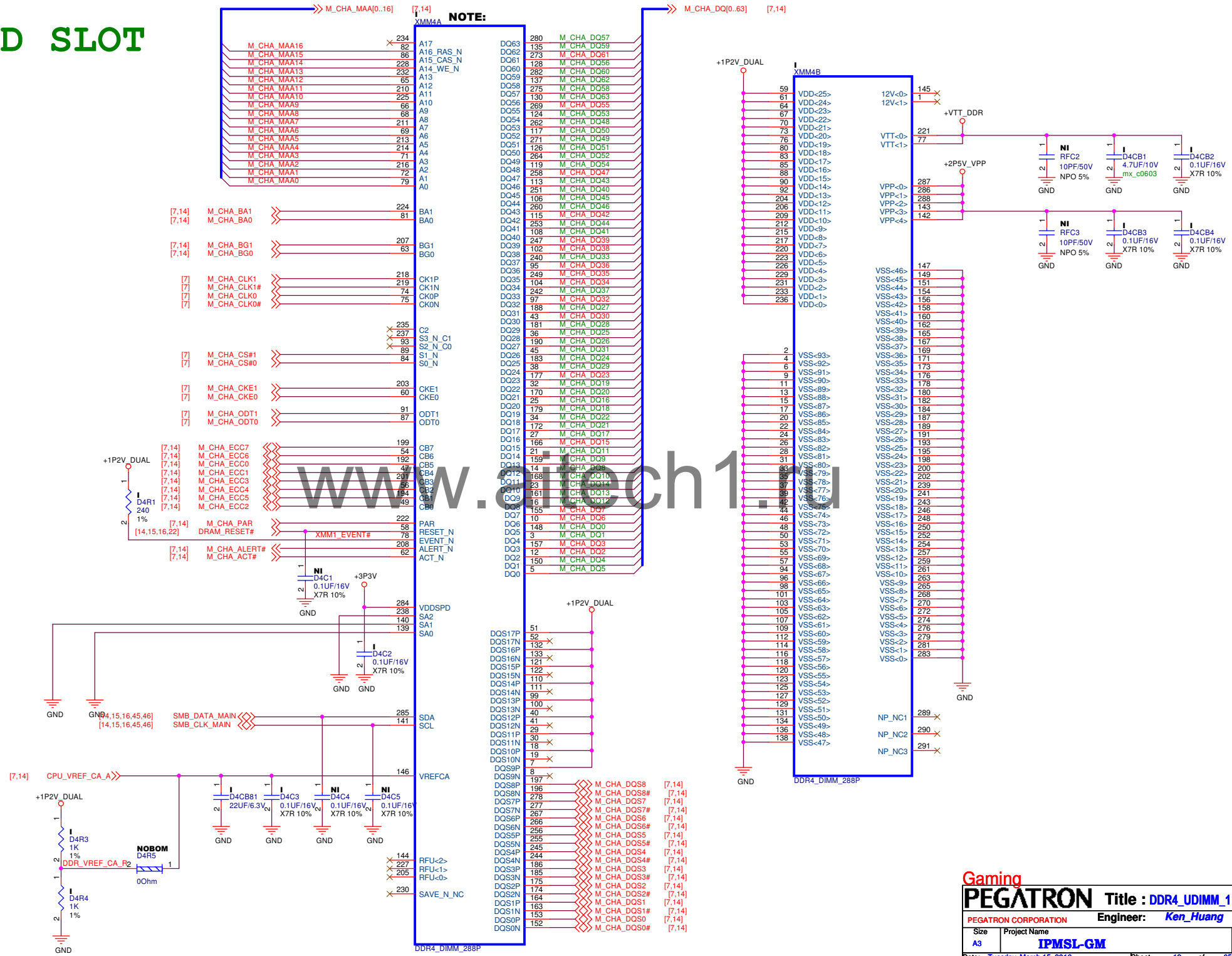




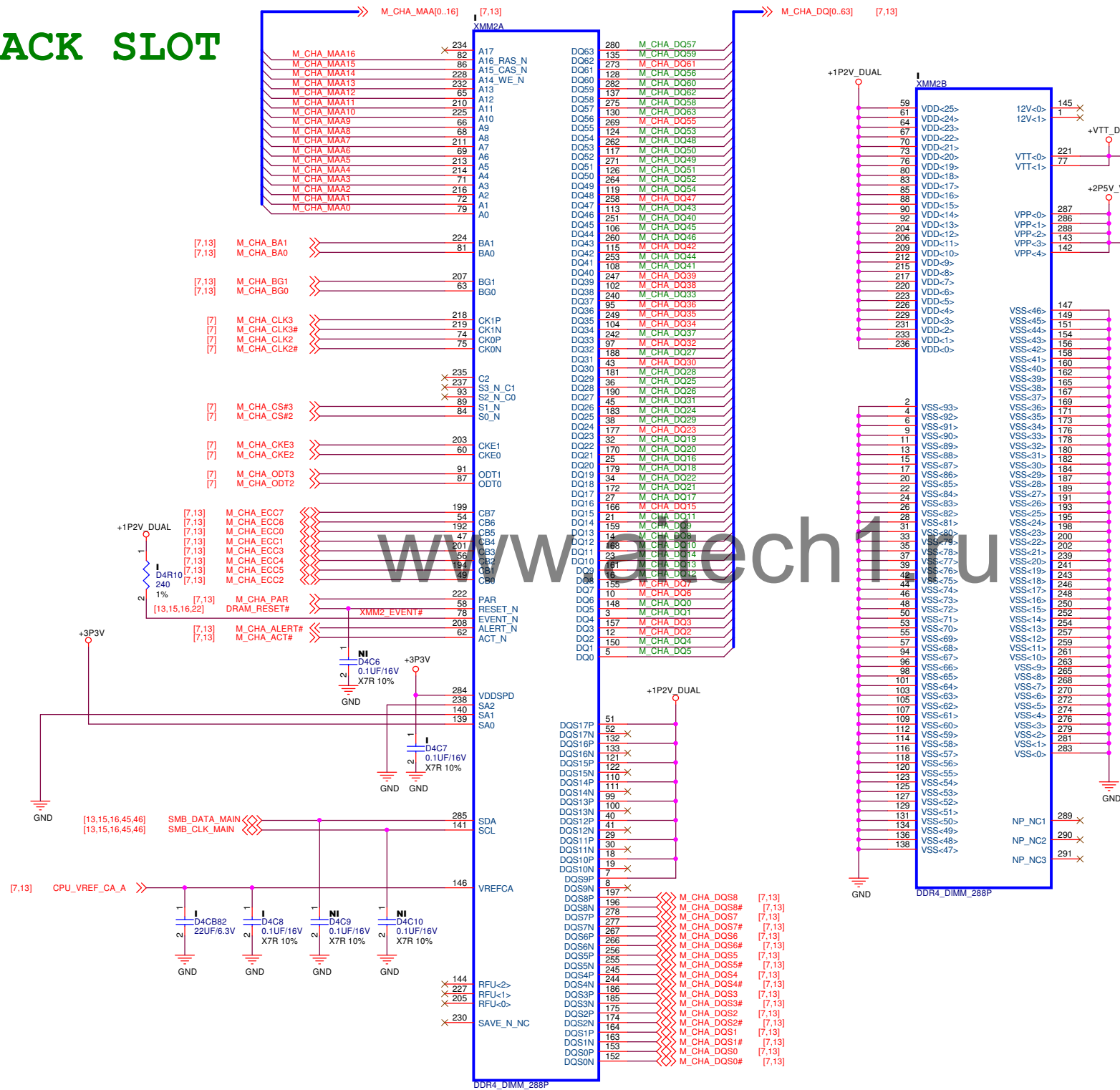




## RED SLOT



## BLACK SLOT

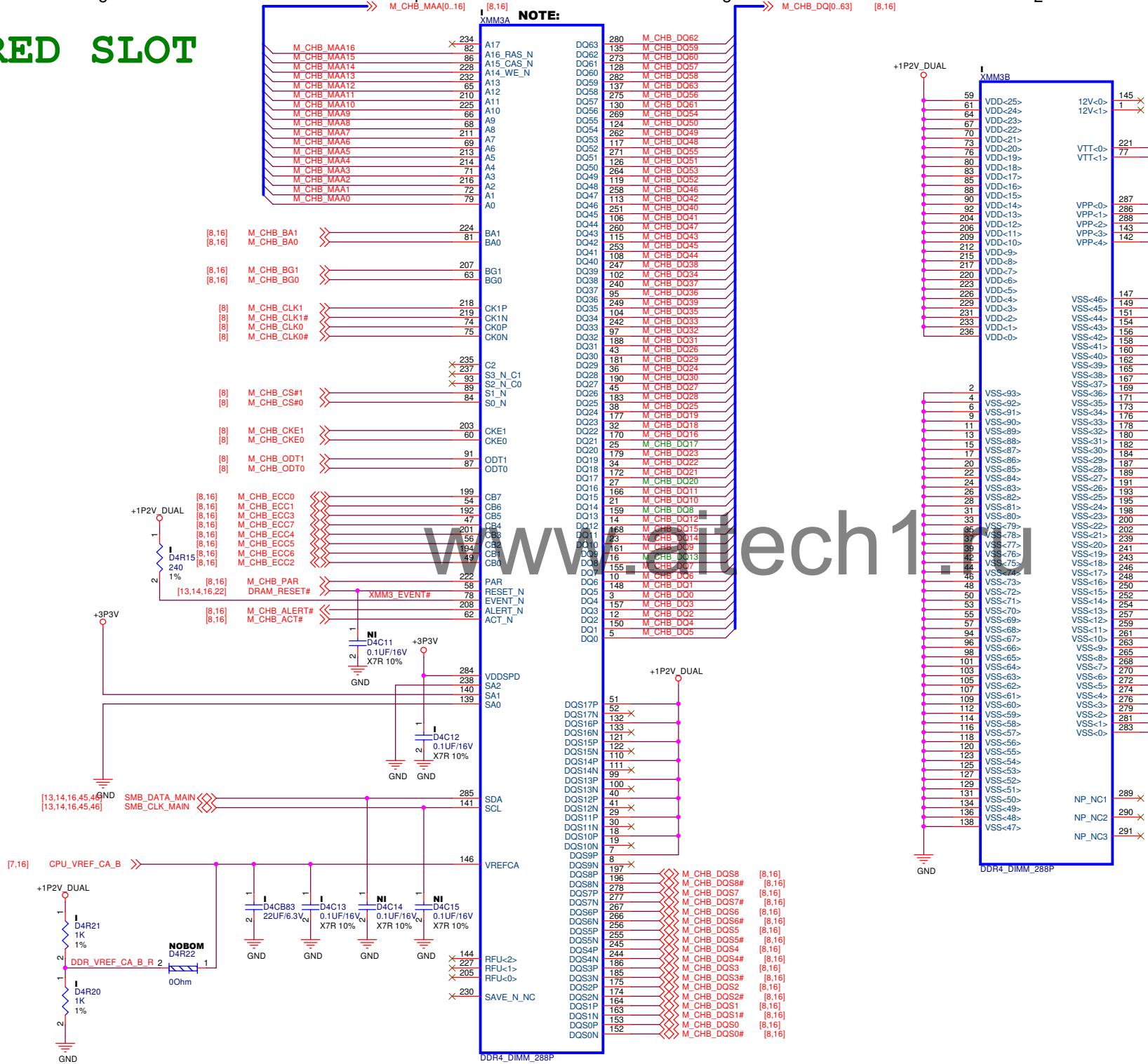


## Gaming

**PEGATRON** Title : **DDR4\_UDIMM\_2**

<b>PEGATRON CORPORATION</b>		<b>Engineer:</b> <i>Ken_Huang</i>	
Size <b>A3</b>	Project Name <b>IPMSL-GM</b>	Rev <b>R1.01</b>	
Date: <b>Tuesday, March 15, 2016</b>		Sheet <b>14</b> of <b>65</b>	

## RED SLOT



## Gaming

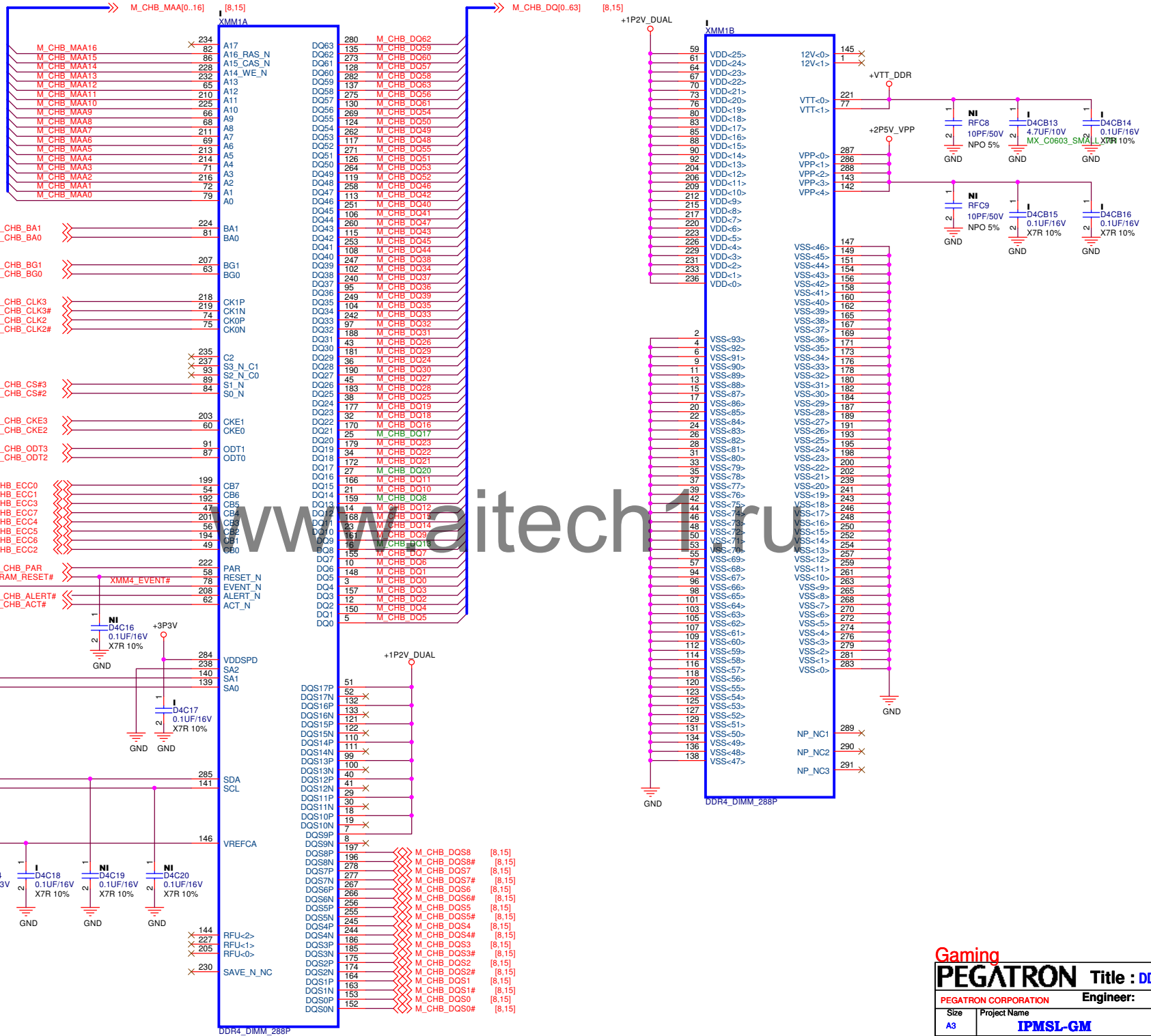
**PEGATRON** Title : DDR4\_UDIMM\_3

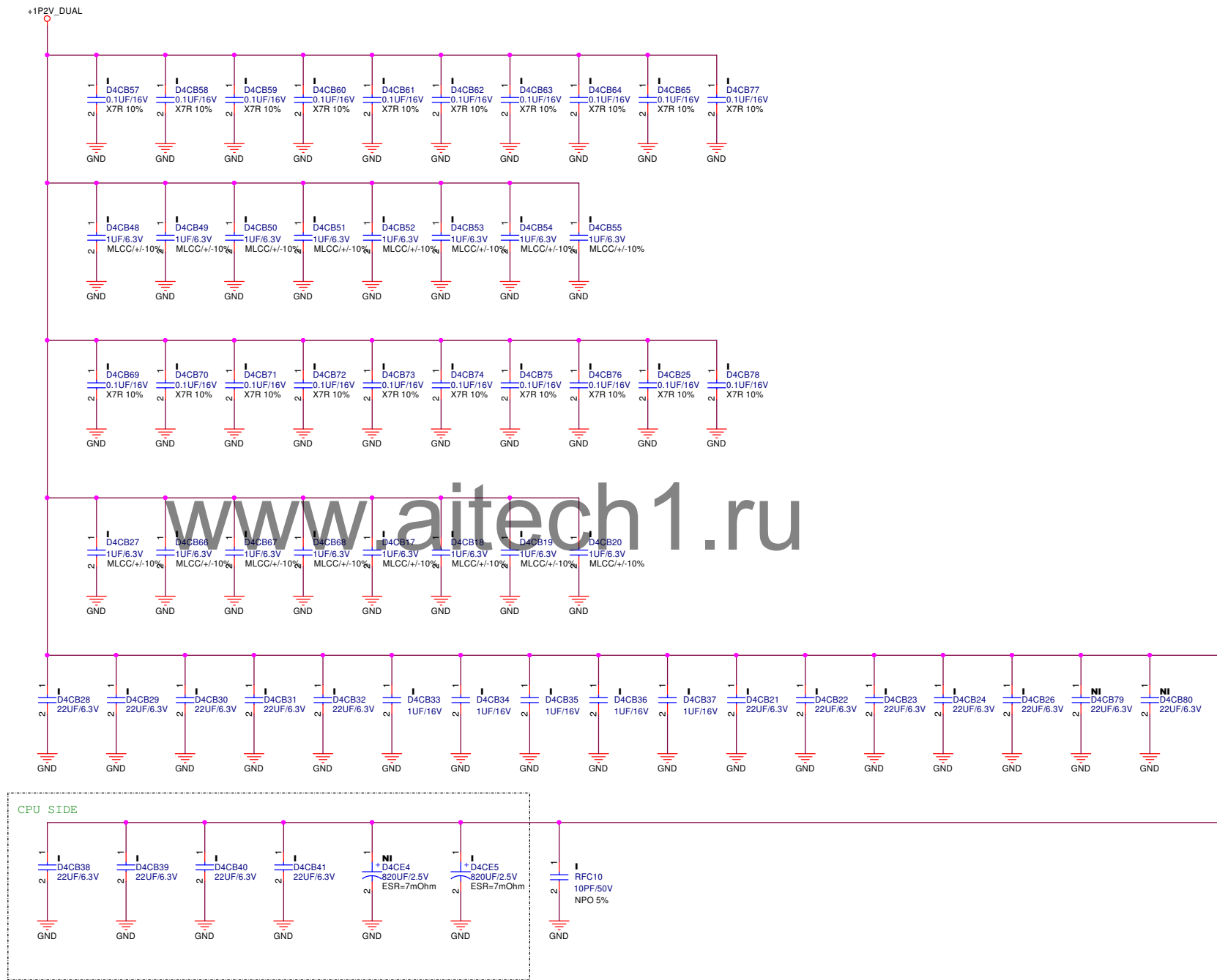
PEGATRON CORPORATION      Engineer:      *Ken\_Huang*

Size <b>A3</b>	Project Name <b>IPMSL-GM</b>	Rev <b>R1.01</b>
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Date: Tuesday, March 15, 2016 Sheet 15 of 65

# BLACK SLOT





U3A

DMI

USB2 . 0



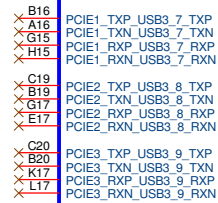
Rear USB3.0

Front USB3.0 CHARGER

Rear RJ45 USB 3.0

M.2 KEY A BLUETOOTH

PCIE/USB/ SATA



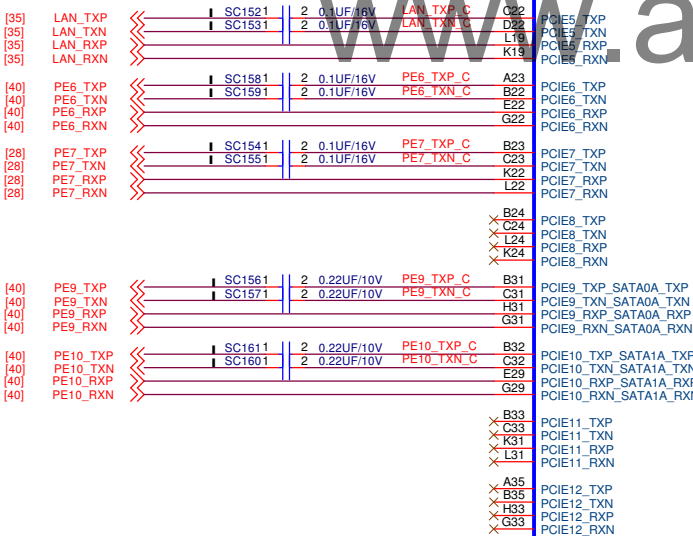
USB3 . 0

LAN

CR REDRIVER

M.2 Key A WIFI

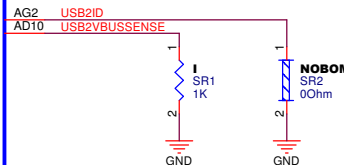
USB3.1 REDRIVER



Rear USB3.0

Rear RJ45 + USB3.0

Front USB3.0

USB2\_ID  
USB2\_VBUSSENSE

SKYLAKE\_PCH

Rev 0.7

Gaming

PEGATRON Title : PCH\_PCIE\_USB\_SATA

PEGATRON CORPORATION Engineer: Ken\_Huang

Size A3 Project Name IPMSL-GM Rev R1.01

Date: Tuesday, March 15, 2016 Sheet 18 of 65



NOTE: DEVSLP

High: requests SATA device to enter into the DEVSLP power state

Low: SATA device to exit from the DEVSLP power state and transition to active state

When used as DEVSLP, no external PU or PD required from SATA Host DEVSLP.

### U3B

#### PCIE/SATA

#### M.2 KEY M SSD

#### SATA Port1

#### SATA Port2

#### SATA Port3

GPP\_E0\_SATAxPCIE0\_SATAGP0  
GPP\_E1\_SATAxPCIE1\_SATAGP1  
GPP\_E2\_SATAxPCIE2\_SATAGP2

GPP\_E3\_CPU\_GP0  
GPP\_E4\_DEVSLP0  
GPP\_E5\_DEVSLP1  
GPP\_E6\_DEVSLP2  
GPP\_E7\_CPU\_GP1  
GPP\_E8\_SATALED\_N

GPP\_E9\_USB2\_OC0\_N  
GPP\_E10\_USB2\_OC1\_N  
GPP\_E11\_USB2\_OC2\_N  
GPP\_E12\_USB2\_OC3\_N

GPP\_F15\_USB2\_OCB\_4  
GPP\_F16\_USB2\_OCB\_5  
GPP\_F17\_USB2\_OCB\_6  
GPP\_F18\_USB2\_OCB\_7

GPP\_I0\_DDPB\_CTRLCLK  
GPP\_I1\_DDPB\_CTRLCLK  
GPP\_I2\_DDPB\_CTRLCLK  
GPP\_I3\_DDPB\_CTRLCLK  
GPP\_I4\_EDP\_HPD

GPP\_I5\_DDPB\_CTRLCLK  
GPP\_I6\_DDPB\_CTRLCLK  
GPP\_I7\_DDPB\_CTRLCLK  
GPP\_I8\_DDPB\_CTRLCLK  
GPP\_I9\_DDPD\_CTRLCLK  
GPP\_I10\_DDPD\_CTRLCLK

GPP\_F0\_SATAxPCIE3\_SATAGP3  
GPP\_F1\_SATAxPCIE4\_SATAGP4  
GPP\_F2\_SATAxPCIE5\_SATAGP5  
GPP\_F3\_SATAxPCIE6\_SATAGP6  
GPP\_F4\_SATAxPCIE7\_SATAGP7

SKYLAKE\_PCH

Rev 0.7

NOTE:

CPU\_GP can be used from external sensors for the thermal management.

NOTE:

Check real OC# application

NOTE:

SATAxPCIE[0:7]	SATA/PCIE
SATAxPCIE0	SATA0A/PCIE9 SATA0B/PCIE13
SATAxPCIE1	SATA1A/PCIE10 SATA1B/PCIE14
SATAxPCIE2	SATA2/PCIE15
SATAxPCIE3	SATA3/PCIE16
SATAxPCIE4	SATA4/PCIE17
SATAxPCIE5	SATA5/PCIE18
SATAxPCIE6	SATA5/PCIE19
SATAxPCIE7	SATA7/PCIE20

NOTE:

GPP\_F[11:10] for SWITCH#0 to select source from ISH or HOST

Gaming

**PEGATRON** Title : PCH\_SATA\_PCIE

PEGATRON CORPORATION Engineer: Ken\_Huang

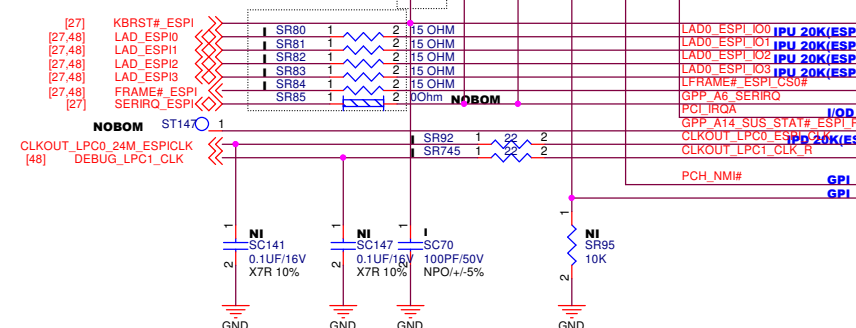
Size A3 Project Name IPMSL-GM Rev R1.01

Date: Tuesday, March 15, 2016 Sheet 19 of 65

eSPI operates at 1.8V

Check SERIRQ & PIRQA volt level

Be carful on LPC/eSPI layout routing  
eSPI clock/data mismatch < 500mil



CLKOUT\_LPC[0:1]  
are 24MHz(TBD)  
with Rs=22ohm

ESPI\_CLK is  
xxHz with  
R<sub>s</sub> = 15ohm

Check PCA spec  
SIO\_SMI# to GPIO  
or SMI#?

TBD; Check ISH GPIO[0:7]

PU/PD and power rail

SPI\_CS2# is dedicated to support TPM on SPI  
SPI interface supports either 3.3V or 1.8V.  
Also, SLB9670VQ2.0 support 3.3V or 1.8V.  
Check CLKRUN# power well  
Check external PU on PME#

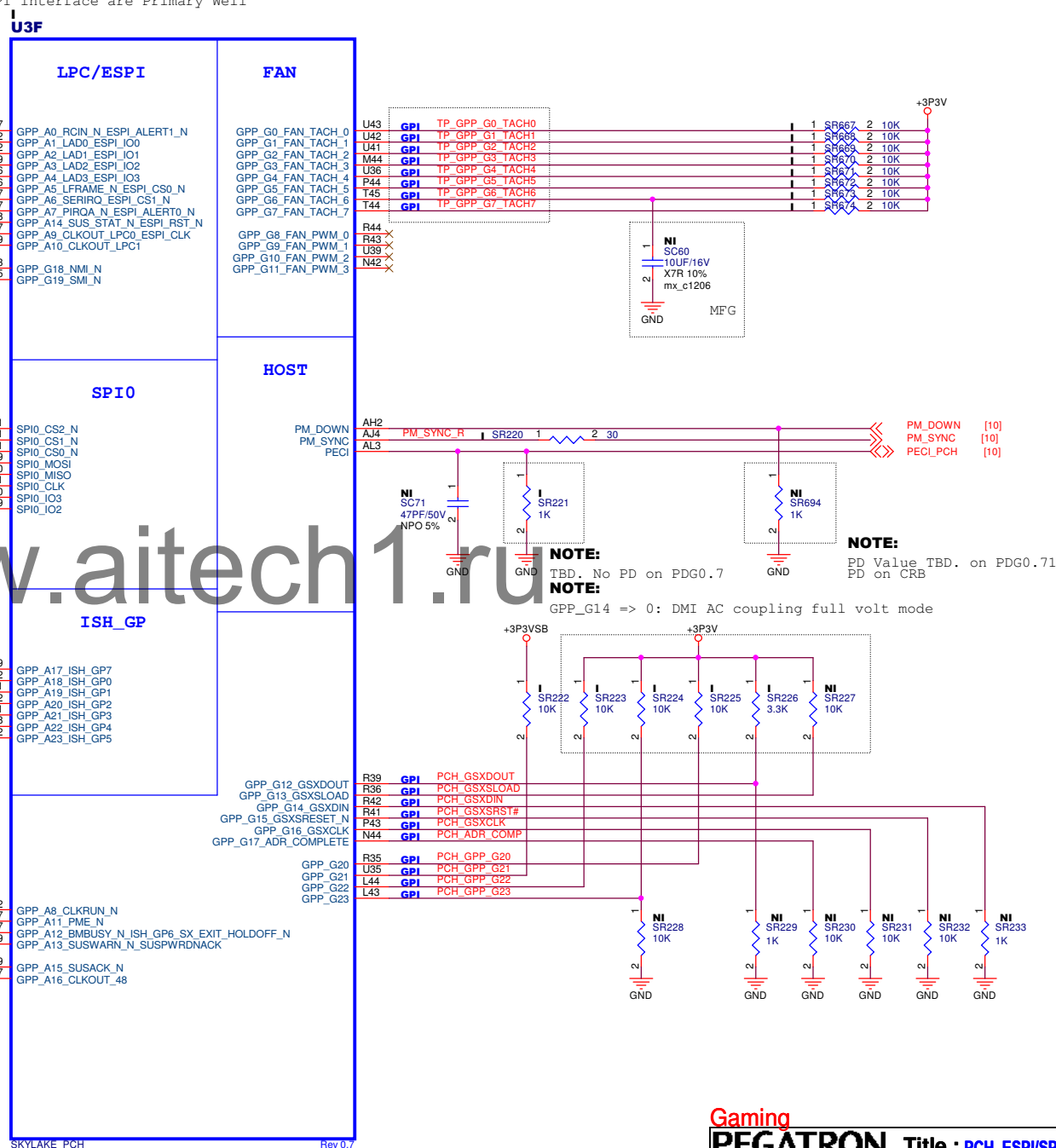
Check USB power rail to decide DSW handshaking

Check GPP\_A0 power well

**NOTE:**

ESPI\_ALERT[0:1]# & ESPI\_CS1# are Server Only  
ESPI interface are Primary Well

Check PCA spec for specific implementation



## Gaming

**PEGATRON** Title : PCH\_ESPI/SPI/FAN

PEGATRON CORPORATION Engineer: *Ken\_Huang*

Size	Project Name	Re
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A3	<b>IPMSL-GM</b>	R1
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Date: Tuesday, March 15, 2016 Sheet 20 of 65





NOTE:

GPP\_B22/GSPI1\_MOSI

Offset 3410h:Bit 10

0: SPI

1: LPC

NOTE:

GSPI is not the same as SPI

It's used mainly for sensor

NOTE:

GSPI0\_MOSI/GPP\_B18

0 = Disable "No Reboot" mode.

1 = Enable "No Reboot" mode

(PCH will disable the TCO Timer system reboot feature).

NOTE:

HP PCA spec request probe points

NOTE:

1.DRAM\_RESET# used on DDR3L, DDR4. Not applicable to LPDDR3

2.Check PCA spec if we need isolation CKT

since DRAM\_RESET# is changed from SHB processor to SKL PCH assertion

3.Also be careful while changing push-pull to OD

4. PU 475ohm on Zumba Beach CRB 0.5

NOTE:

PCH\_PWROK and  
VCCST\_PWROK have  
the same timing

U3D

GSPI

ISH\_I2C

SKYLAKE\_PCH

Rev.0.7

NOTE:

Check PCH PLL VSB(PRIM) and GPIO PU(GPO) MAIN power  
W/O IPD 20Kohm.

Ex: GPP\_B11

NOTE:

SML[2:4] are Server Only

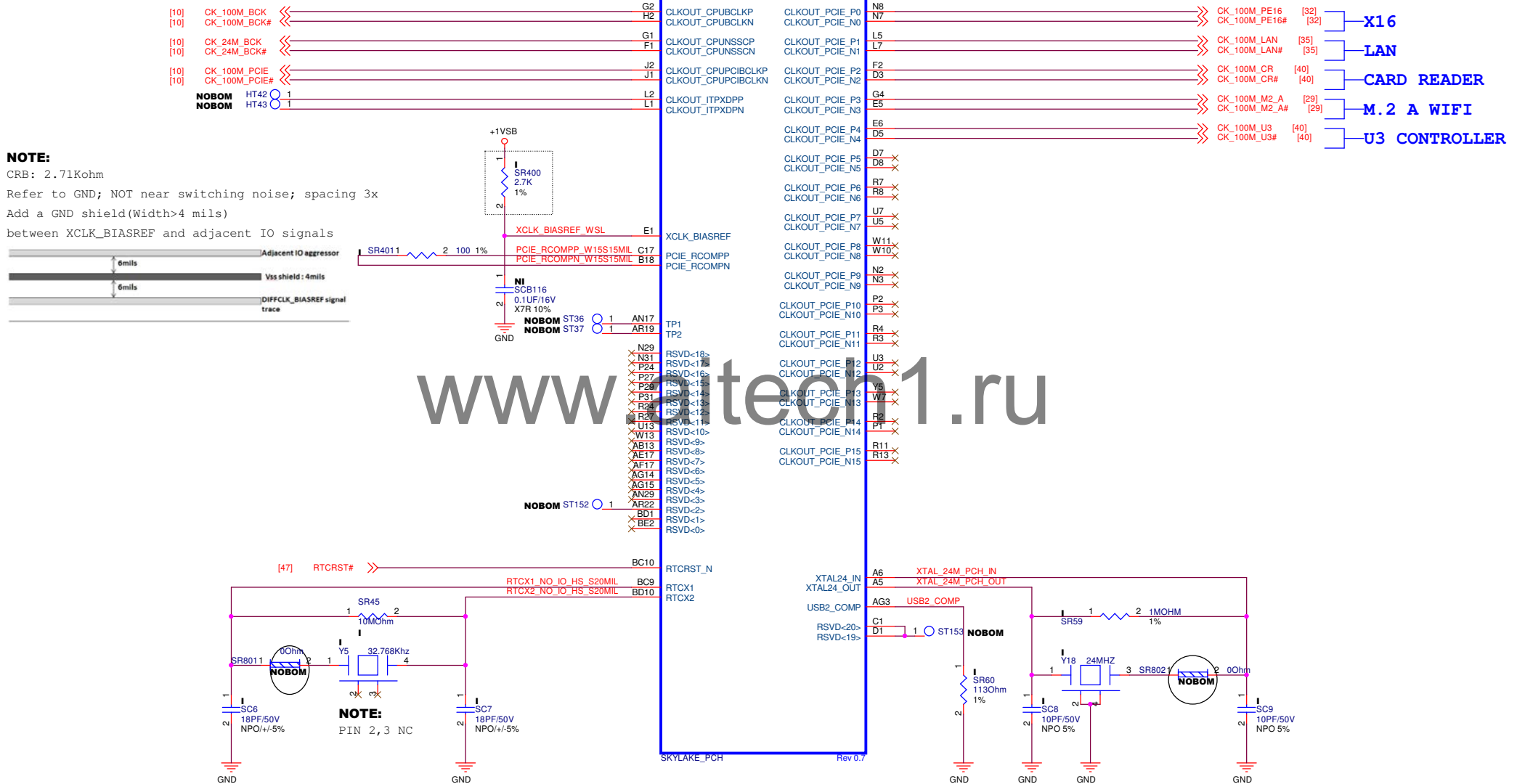
Gaming

PEGATRON Title : PCH\_SML/MISC

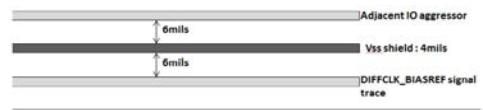
PEGATRON CORPORATION Engineer: Ken\_Huang

Size A3 Project Name IPMSL-GM Rev R1.01

Date: Tuesday, March 15, 2016 Sheet 22 of 65



**NOTE:**  
CRB: 2.71Kohm  
Refer to GND; NOT near switching noise; spacing 3x  
Add a GND shield(Width>4 mils)  
between XCLK\_BIASREF and adjacent IO signals



**NOTE:**  
PIN 2, 3 NC

D

**NOTE:**  
Add 2x 22uF (instead of 47uF) 0603 caps  
on 3.3V/1.8V/1.0V plane at PCH  
Check 22uF qty on power CKT

C

**NOTE:**  
Reserve 0 ohm/0603 for 2.2uH Series Inductor

B

A

$I_{cc(max)} : 6.15A$

$I_{cc(max)} : 0.341A (VCCCLKx \text{ total})$

$I_{cc(max)} : 0.062A$

**NOTE:**  
Place to U3.A43

$I_{cc(max)} : 0.021A$

for noise in 5G  
WiFi band

SKYLAKE\_PCH

Rev 0.7

U3G

PRIMARY

VCCPRIM\_1P0<12>  
VCCPRIM\_1P0<16>  
VCCPRIM\_1P0<15>  
VCCPRIM\_1P0<14>  
VCCPRIM\_1P0<13>  
VCCPRIM\_1P0<11>  
VCCPRIM\_1P0<10>  
VCCPRIM\_1P0<9>  
VCCPRIM\_1P0<8>  
VCCPRIM\_1P0<7>  
VCCPRIM\_1P0<6>  
VCCPRIM\_1P0<5>  
VCCPRIM\_1P0<4>  
VCCPRIM\_1P0<3>  
VCCPRIM\_1P0<2>  
VCCPRIM\_1P0<1>  
VCCPRIM\_1P0<0>

CLOCK

VCCCLK5<0>  
VCCCLK5<1>  
VCCCLK1  
VCCCLK3  
VCCCLK4  
VCCCLK2  
VCCCLK6

MPHY

VCCMPHY\_1P0<1>  
VCCMPHY\_1P0<2>  
VCCMPHY\_1P0<3>  
VCCMPHY\_1P0<4>  
VCCMPHY\_1P0<0>  
VCCMPHYPLL\_1P0<1>  
VCCMPHYPLL\_1P0<0>  
VCCPCIESPLL\_1P0<1>  
VCCPCIESPLL\_1P0<0>

PRIMARY

VCCPRIM\_3P3<3>  
VCCPRIM\_3P3<4>  
VCCPRIM\_3P3<2>  
VCCPRIM\_3P3<0>

VCCRTOPRIM\_3P3  
VCCRTOPRIM\_3P3<0>

VCCATS

VCCDSW\_3P3<1>  
VCCDSW\_3P3<0>

VCCHDA

VCCRTC

VCCGPIO

VCCGPPA

VCCGPPPBCH1  
VCCGPPPBCH2  
VCCGPPPEF<1>  
VCCGPPPEF<0>  
VCCGPPPG

VCCGPPD4  
VCCGPPD3  
VCCGPPD2  
VCCGPPD1

SPI

VCCSPI<2>  
VCCSPI<0>  
VCCSPI<1>

NOTE:

Check real GPIO implementation to decide VccGPIO rail is 3.3V or 1.8V

$I_{cc(max)} : 0.088A (3.3V) / 0.053A (1.8V)$

NOTE:

Place 0.1uF near U3.BC42/ AJ41/ AD41 pins

$I_{cc(max)} : 0.013A (3.3V) / 0.008A (1.8V)$

NOTE:

1.8V SPI (with Quad IO) is expensive than 3.3V part.

$I_{cc(max)} : 0.37A$

$I_{cc(max)} : 0.001A$

NOTE:

Place 0.1uF near U3.AN5

$I_{cc(max)} : 0.007A$

$I_{cc(max)} : 0.502A$

$I_{cc(max)} : 0.075A (3.3V) / 0.045A (1.8V) W10MIL$

$I_{cc(max)} : 0.001A$

NOTE:

Add 2x 22uF (instead of 47uF) 0603 caps  
on 3.3V/1.8V/1.0V plane at PCH  
Check 22uF qty on power CKT

NOTE:

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCGPPPBCH	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCGPPD	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCGPPPEF	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCGPPPG	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPRIM_3P3	3.3V
Primary Well Group G (GPP_G)	VCCDSW_3P3	3.3V
Primary Well Group H (GPP_H)		
Primary Well Group I (GPP_I)		
Deep Sleep Well Group (GPD)		

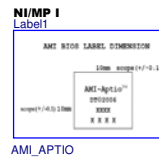
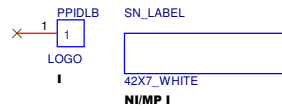
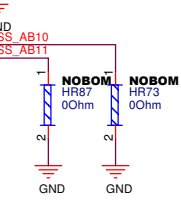
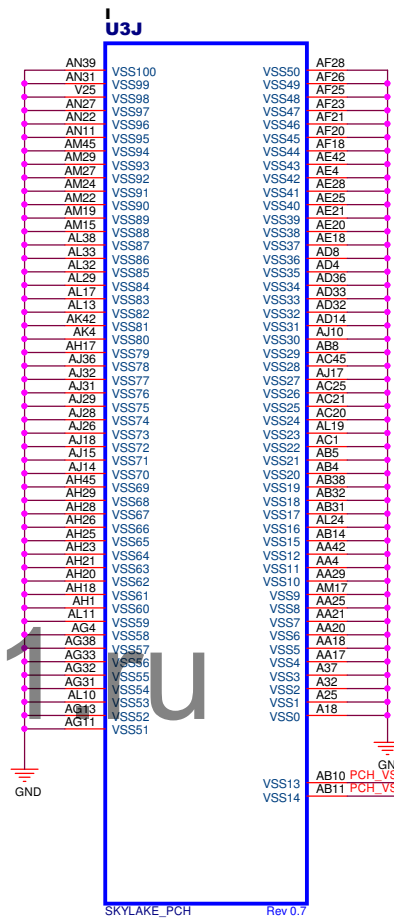
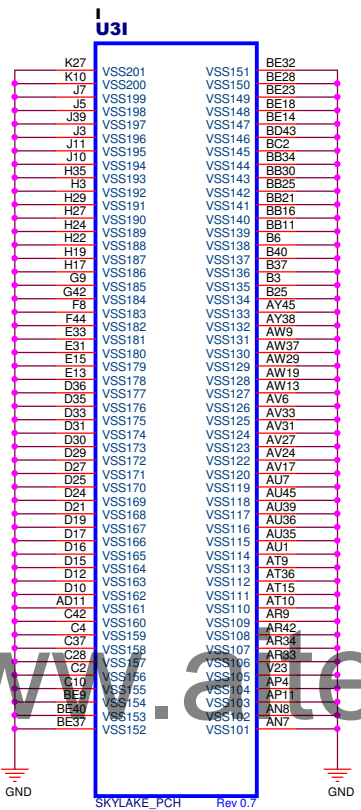
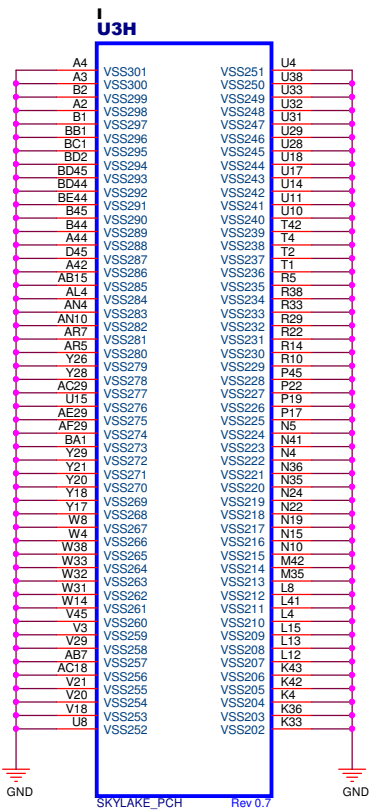
Gaming

**PEGATRON** Title : PCH\_VCC

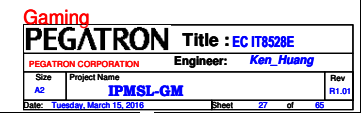
PEGATRON CORPORATION Engineer: Ken\_Huang

Size A3 Project Name IPMSL-GM Rev R1.01

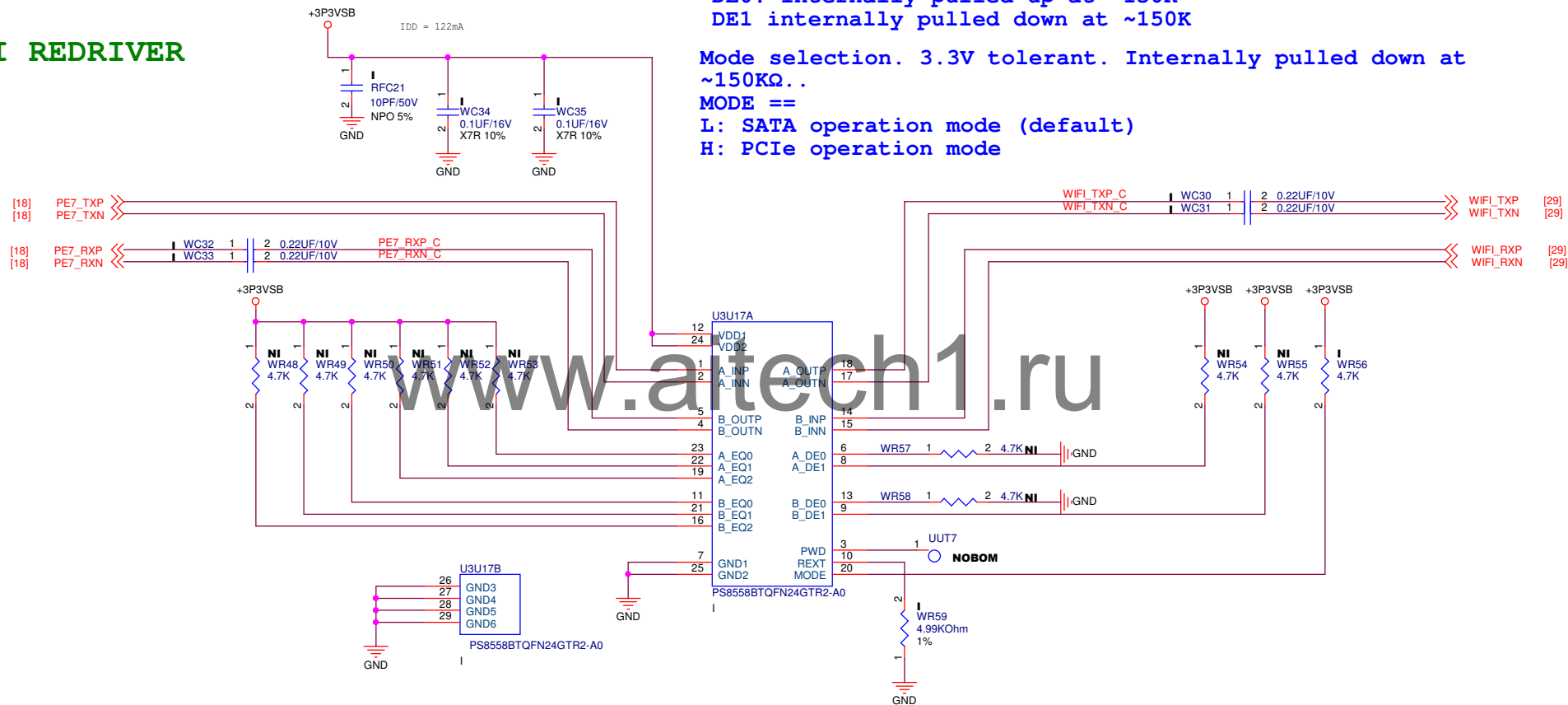
Date: Tuesday, March 15, 2016 Sheet 24 of 65





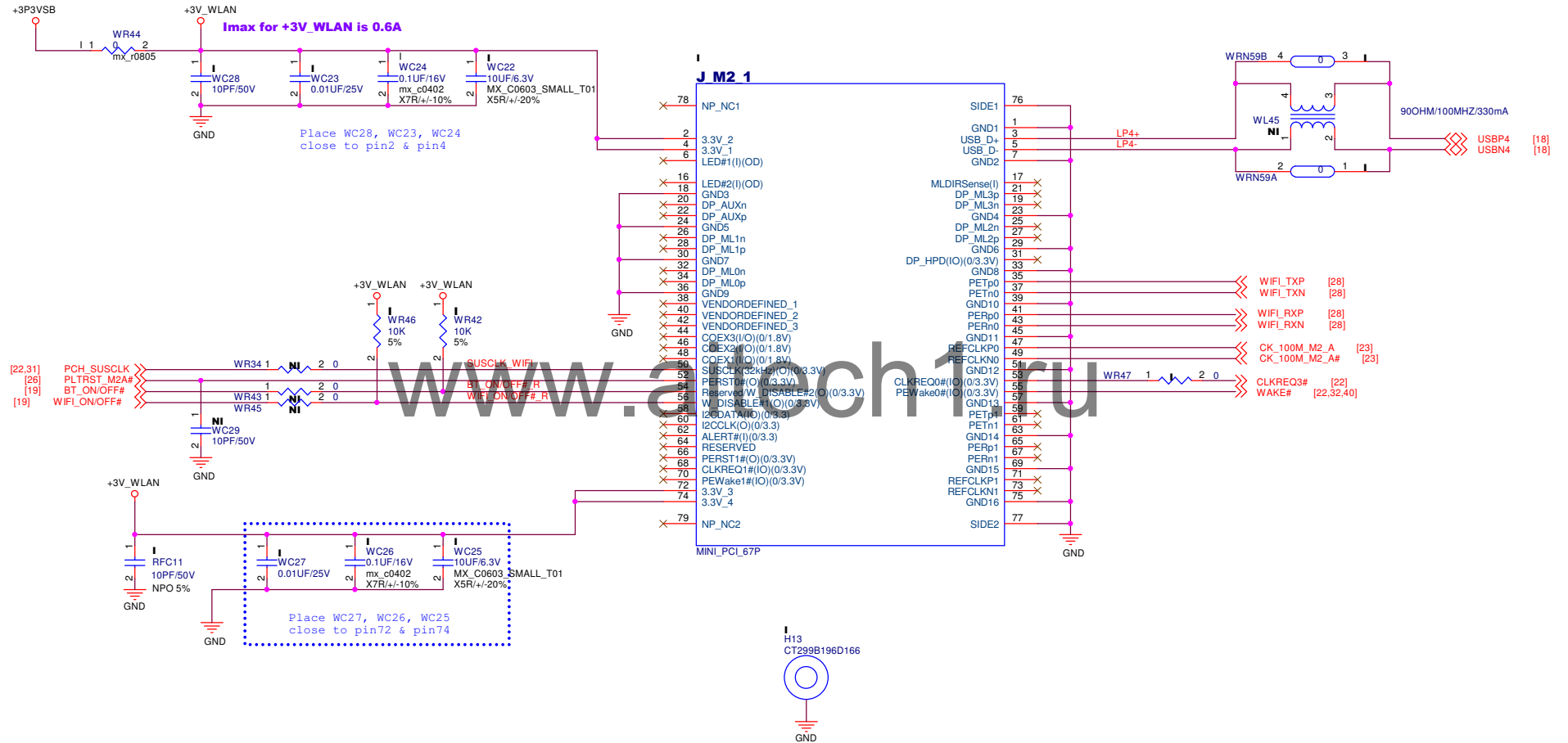


## WIFI REDRIVER

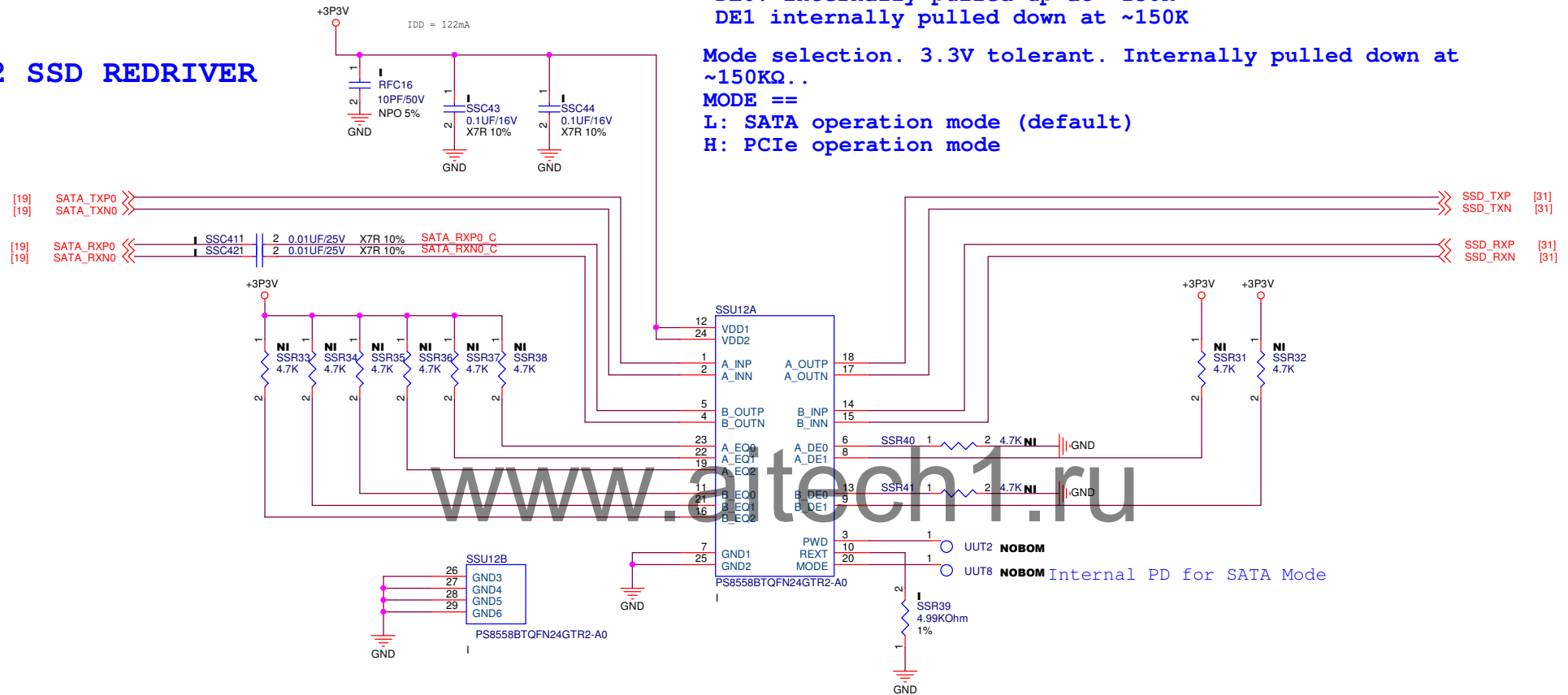




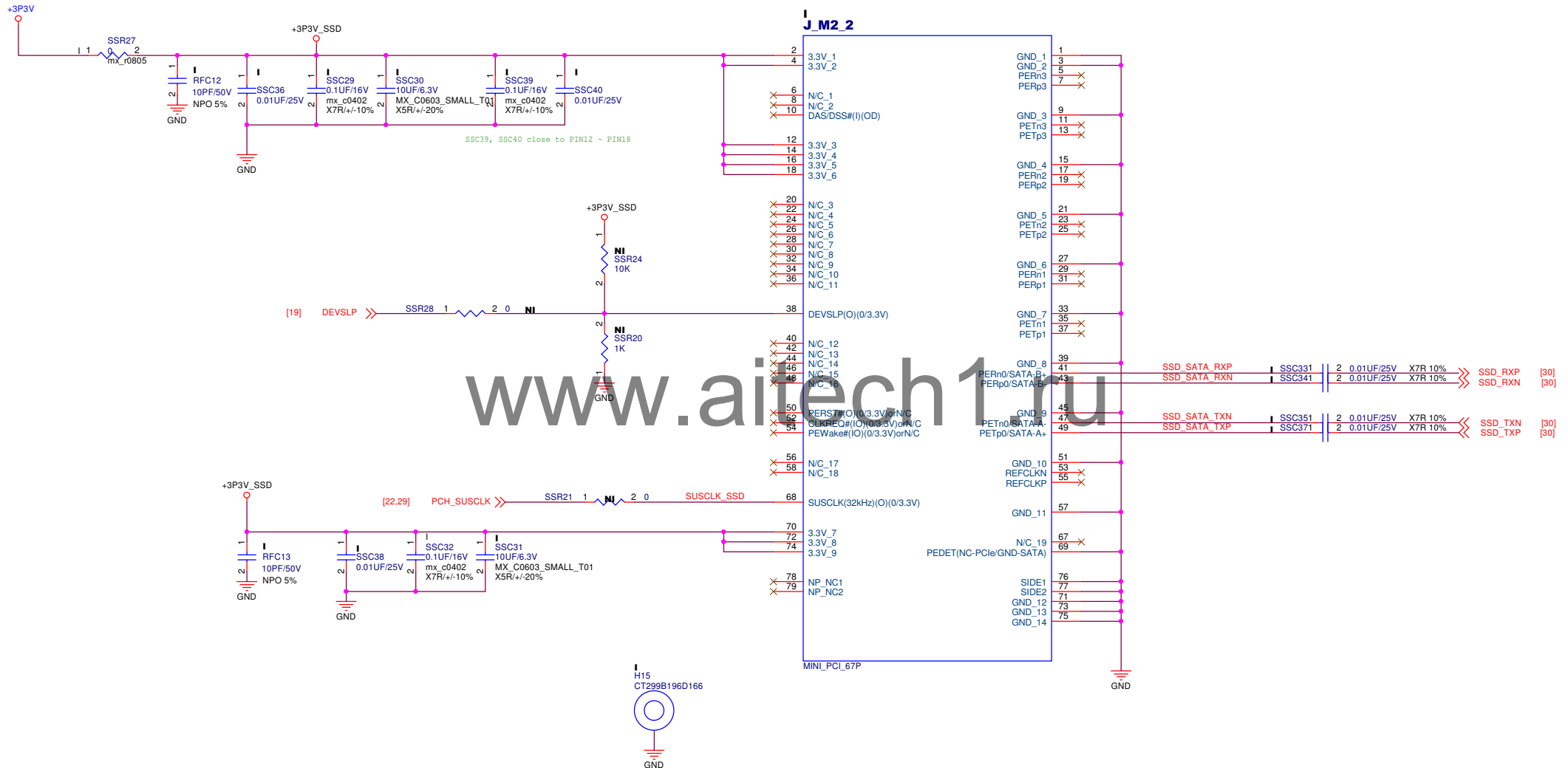
# M.2 WIFI KEY A



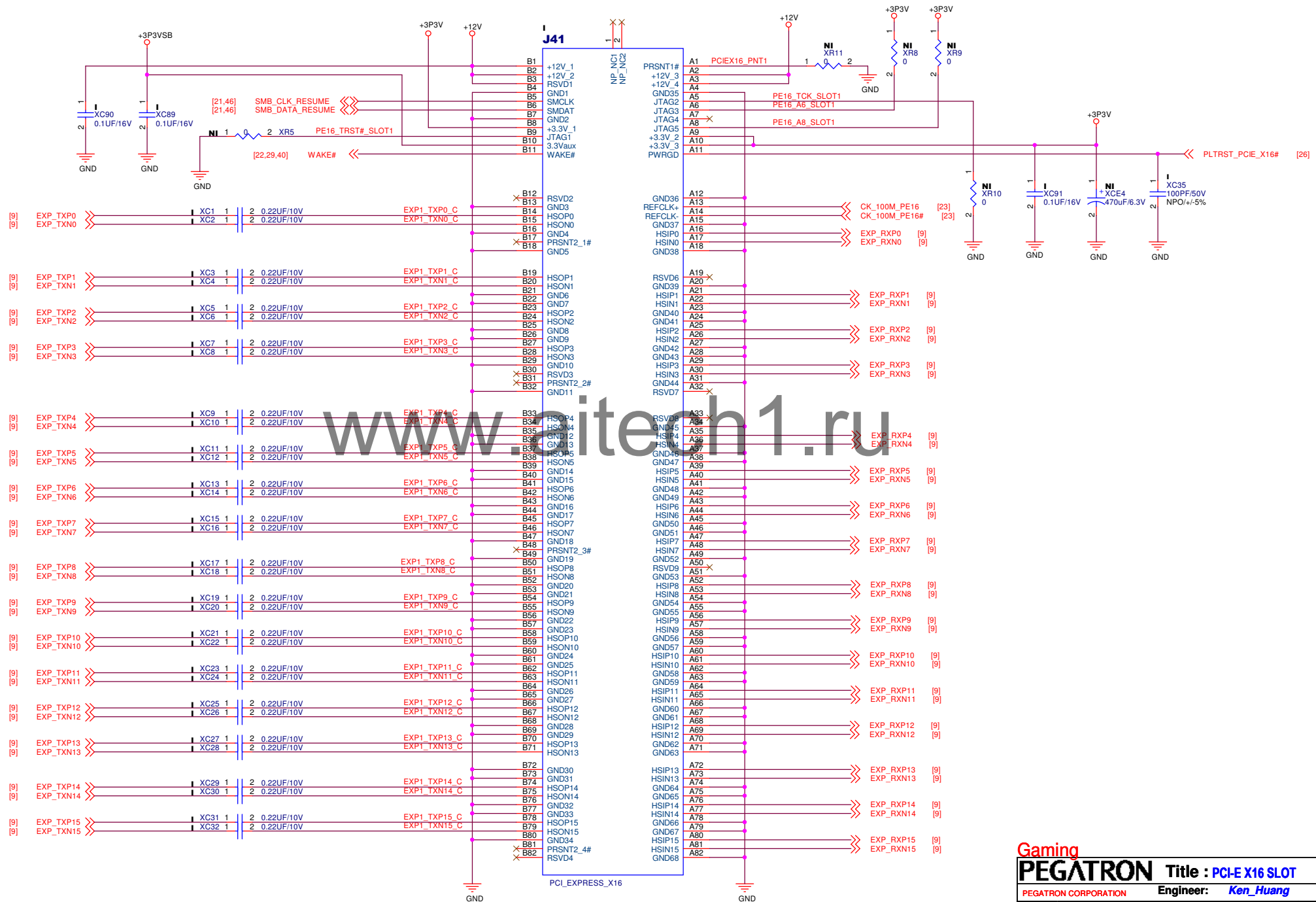
## M2 SSD REDRIVER

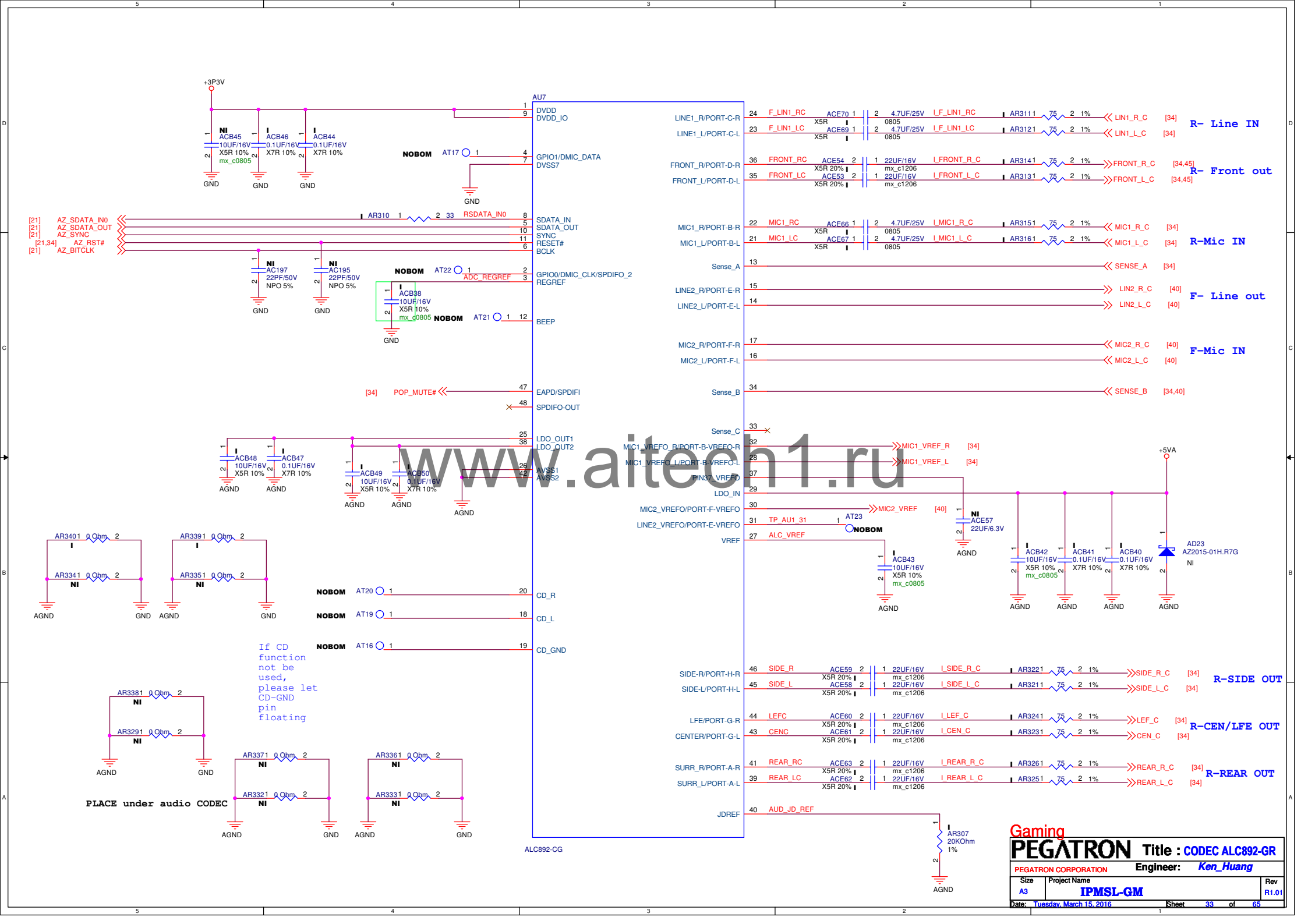


## M.2 SSD KEY M

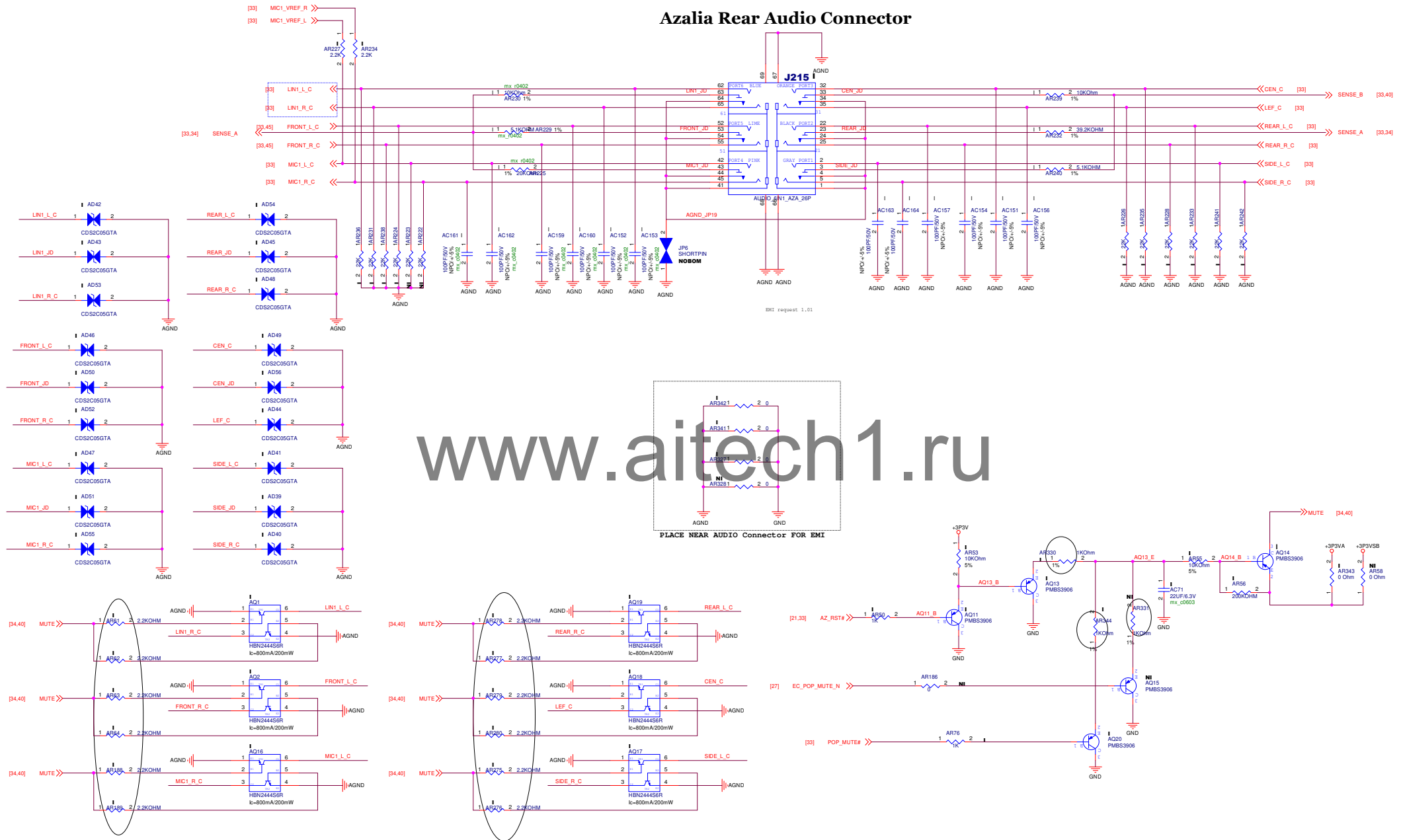


# PCI EXPRESS X16 Graphics Card Slot



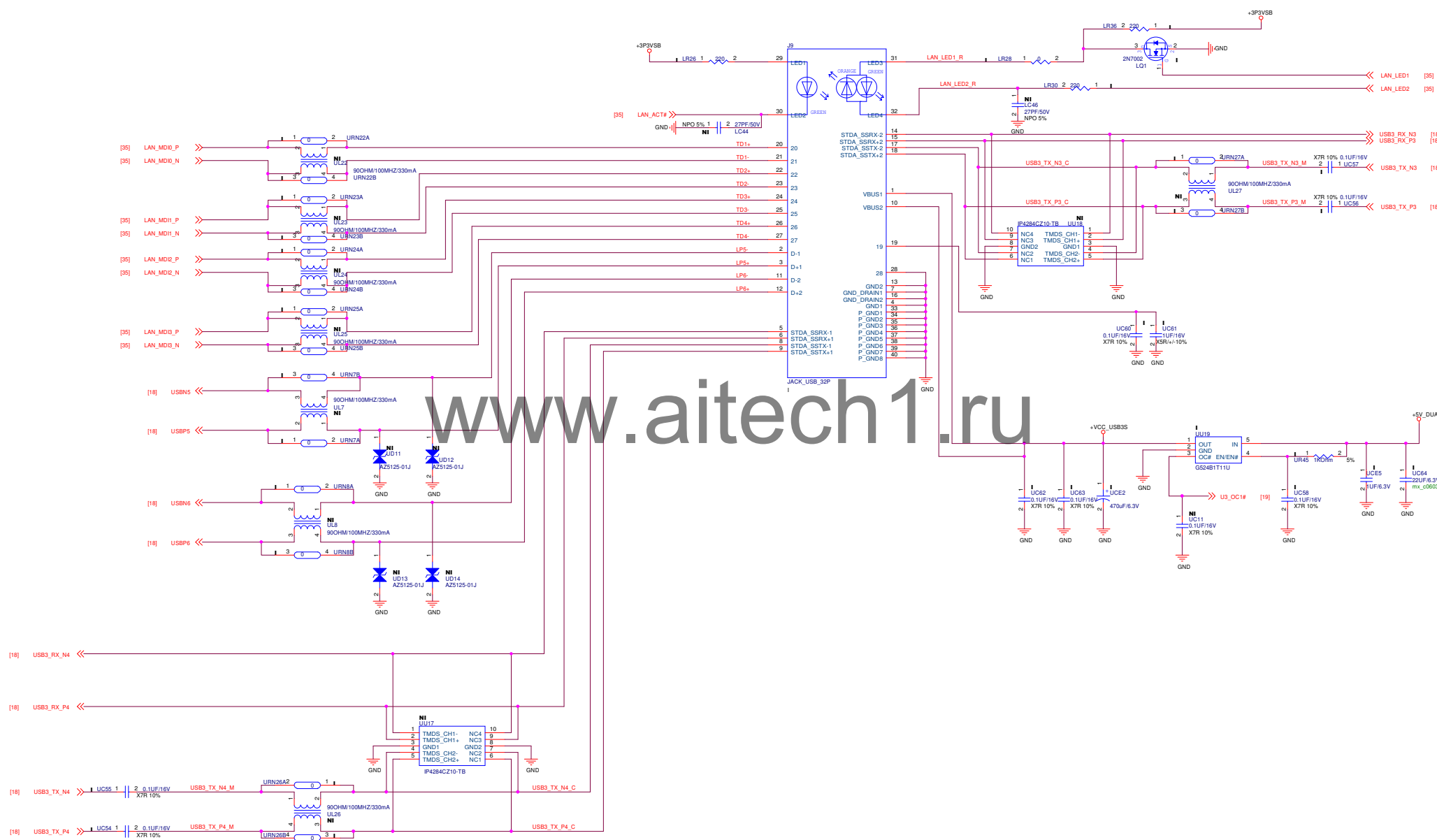


## Azalia Rear Audio Connector

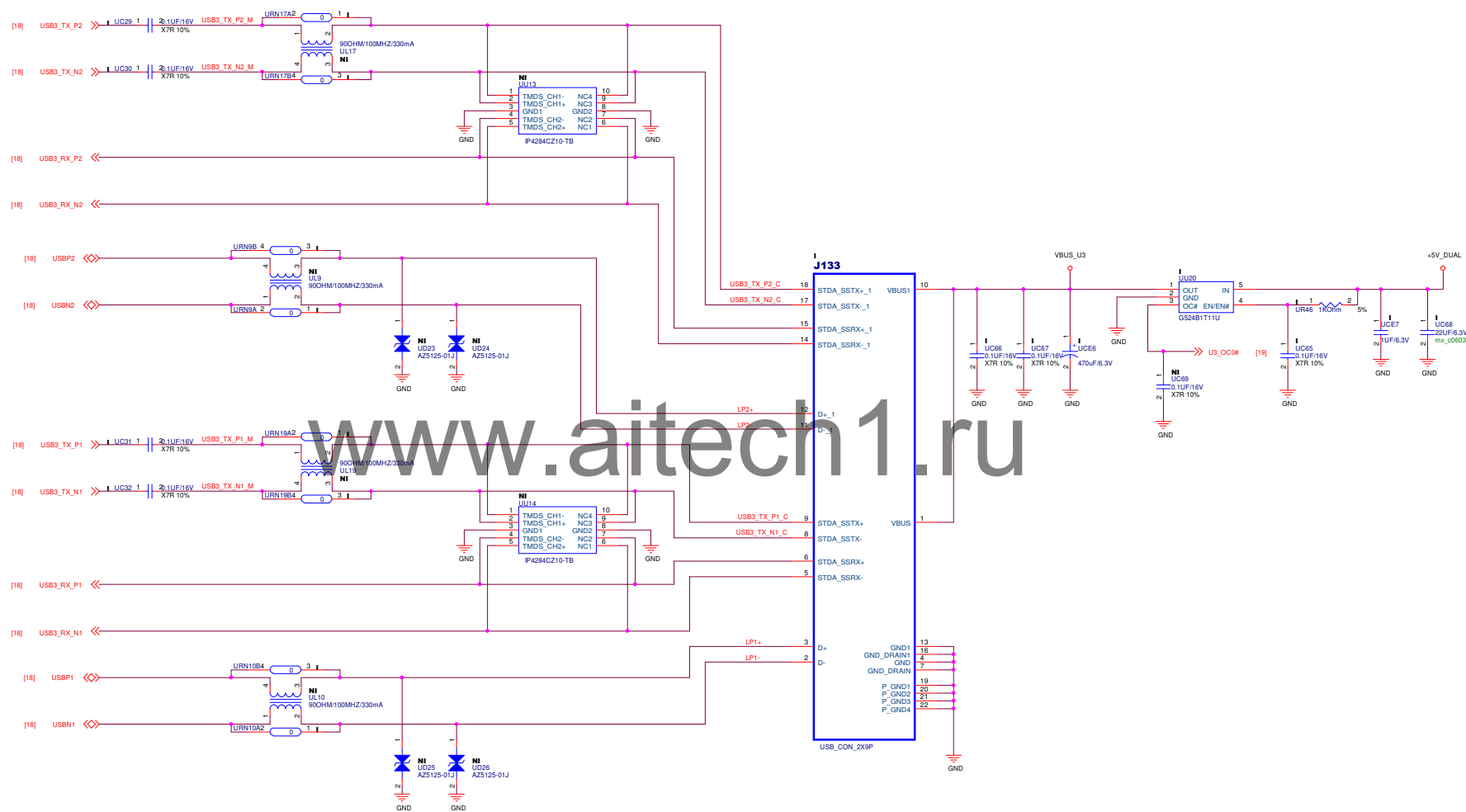


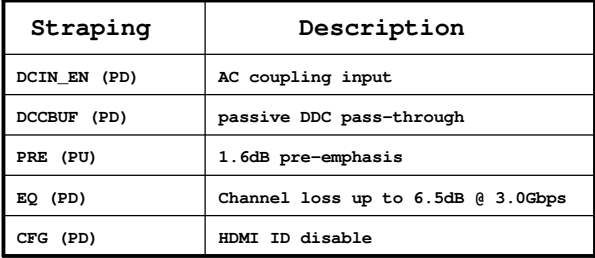


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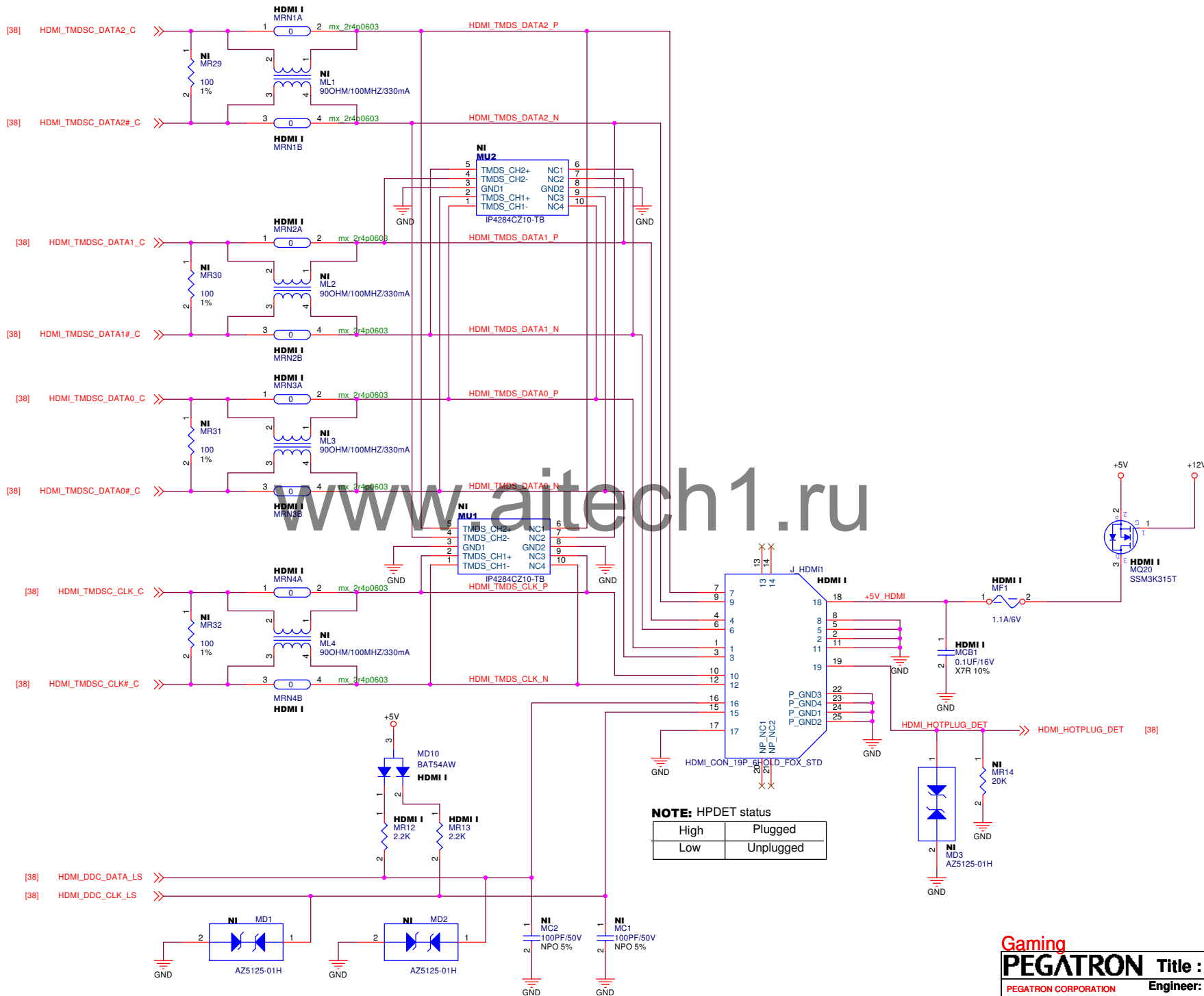
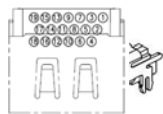


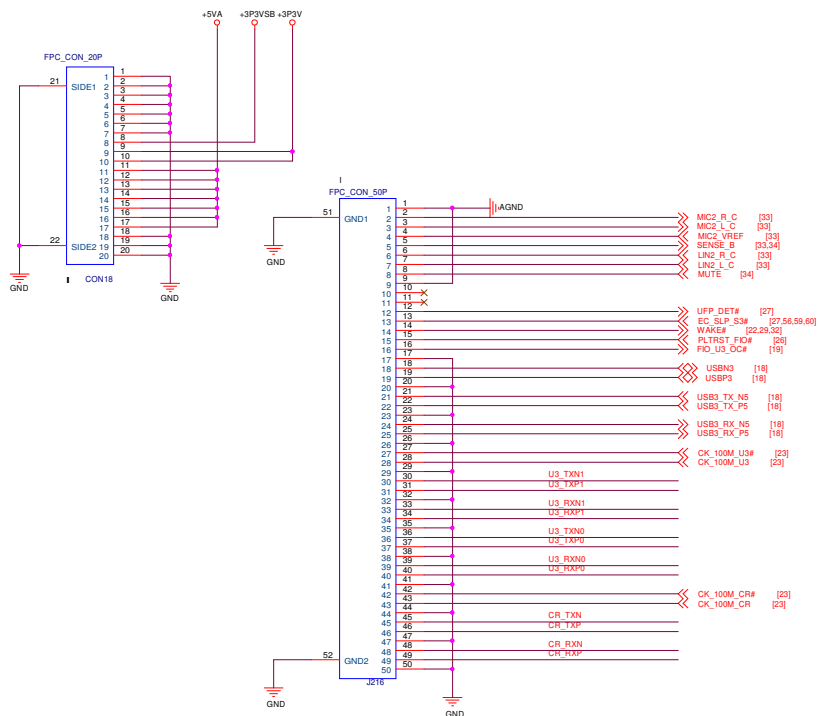






Strapping	Description
I2C_CTL_EN (PD)	Pin Control is selected.
PD# (PU)	Normal operation





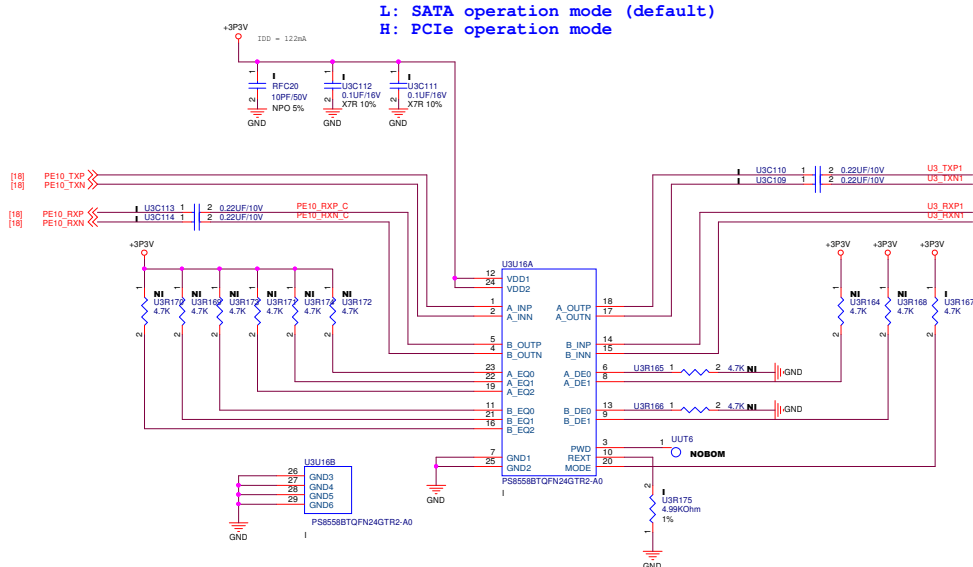
Equalizer control and program for channel A / B  
internally pulled down at ~150K

Programmable output de-emphasis level setting for channel A  
DE0: internally pulled up at ~150K  
DE1 internally pulled down at ~150K

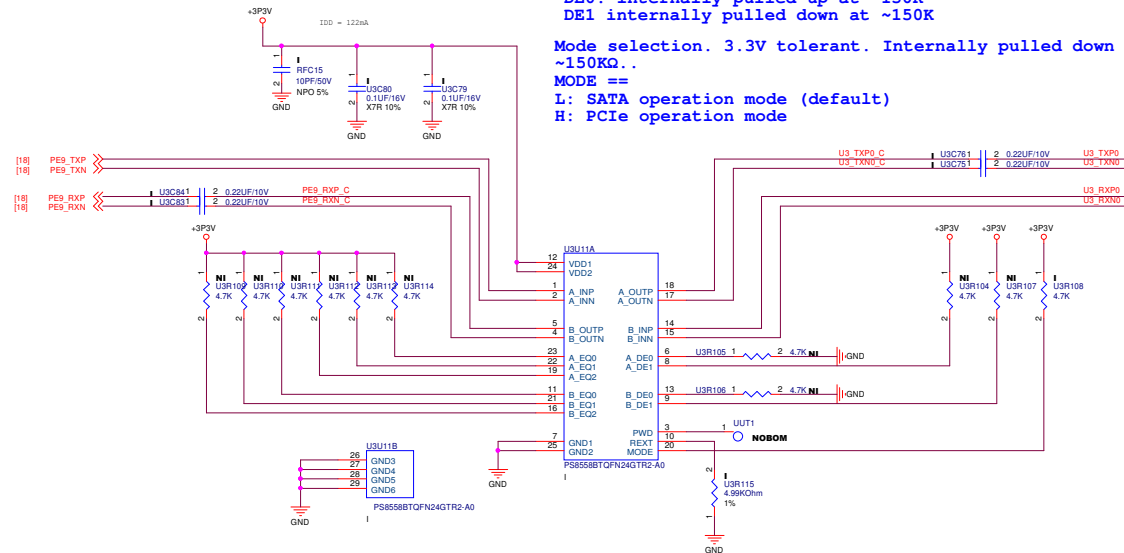
Mode selection. 3.3V tolerant. Internally pulled down at  
~150KΩ..

MODE ==  
L: SATA operation mode (default)  
H: PCIe operation mode

## USB3.1 REDRIVER



## USB3.1 REDRIVER



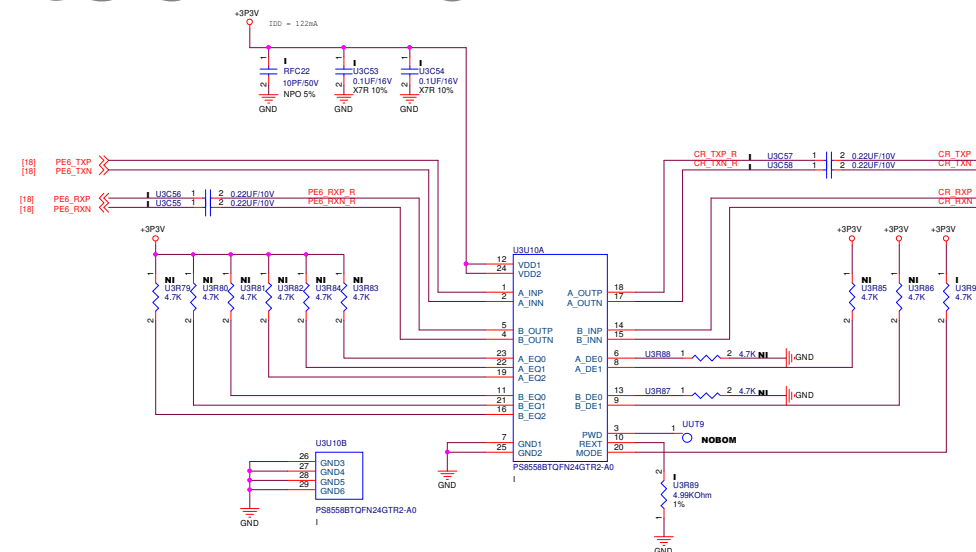
Equalizer control and program for channel A / B  
internally pulled down at ~150K

Programmable output de-emphasis level setting for channel A  
DE0: internally pulled up at ~150K  
DE1 internally pulled down at ~150K

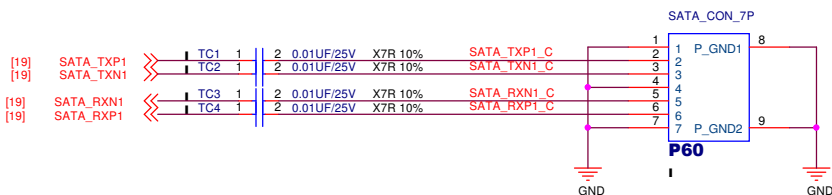
Mode selection. 3.3V tolerant. Internally pulled down at  
~150KΩ..

MODE ==  
L: SATA operation mode (default)  
H: PCIe operation mode

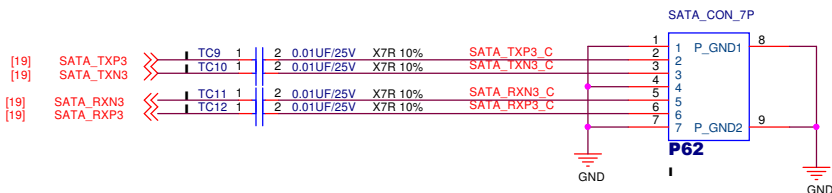
## CR REDRIVER



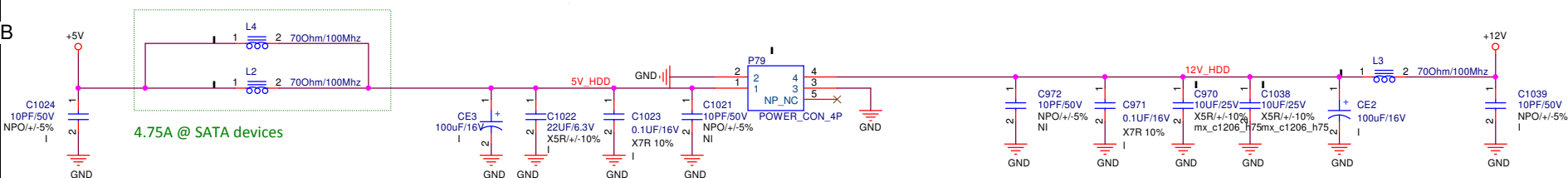
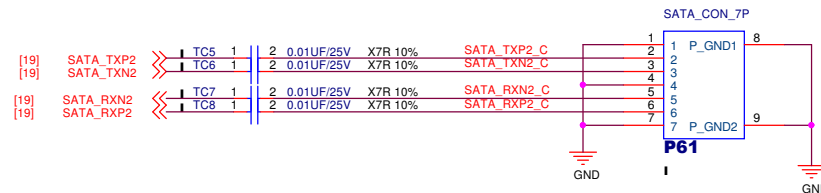
COLOR = RED



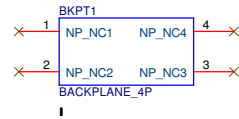
\_\_\_\_\_



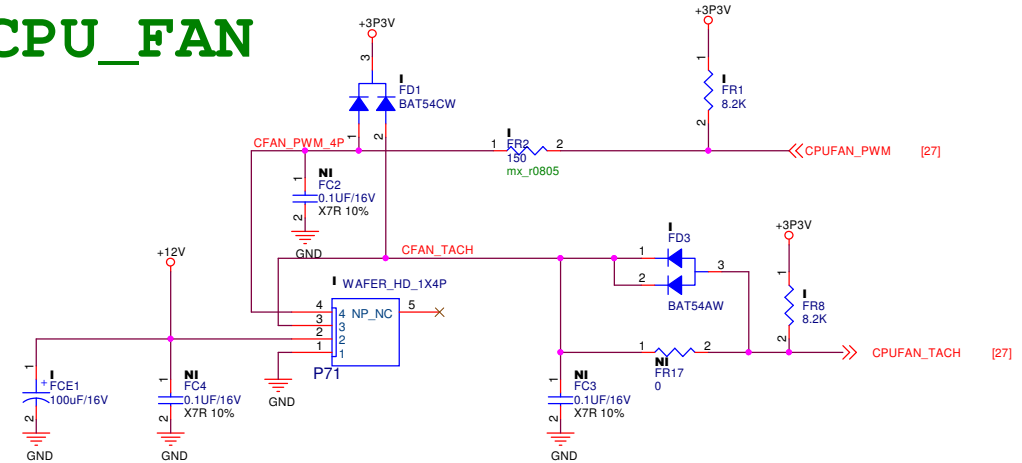
COLOR=RED



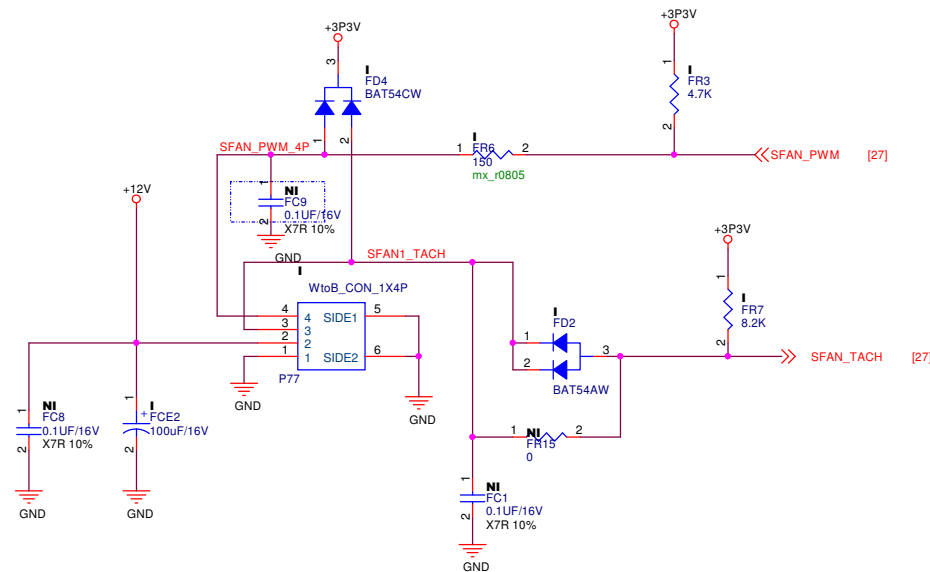
## Back IO for FAN



## CPU\_FAN

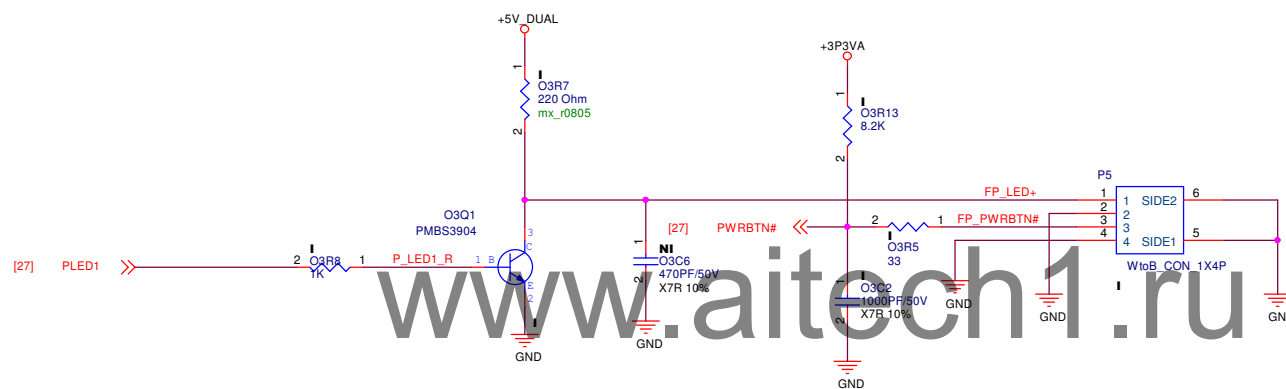


## SYS\_FAN



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## Power Button / LED



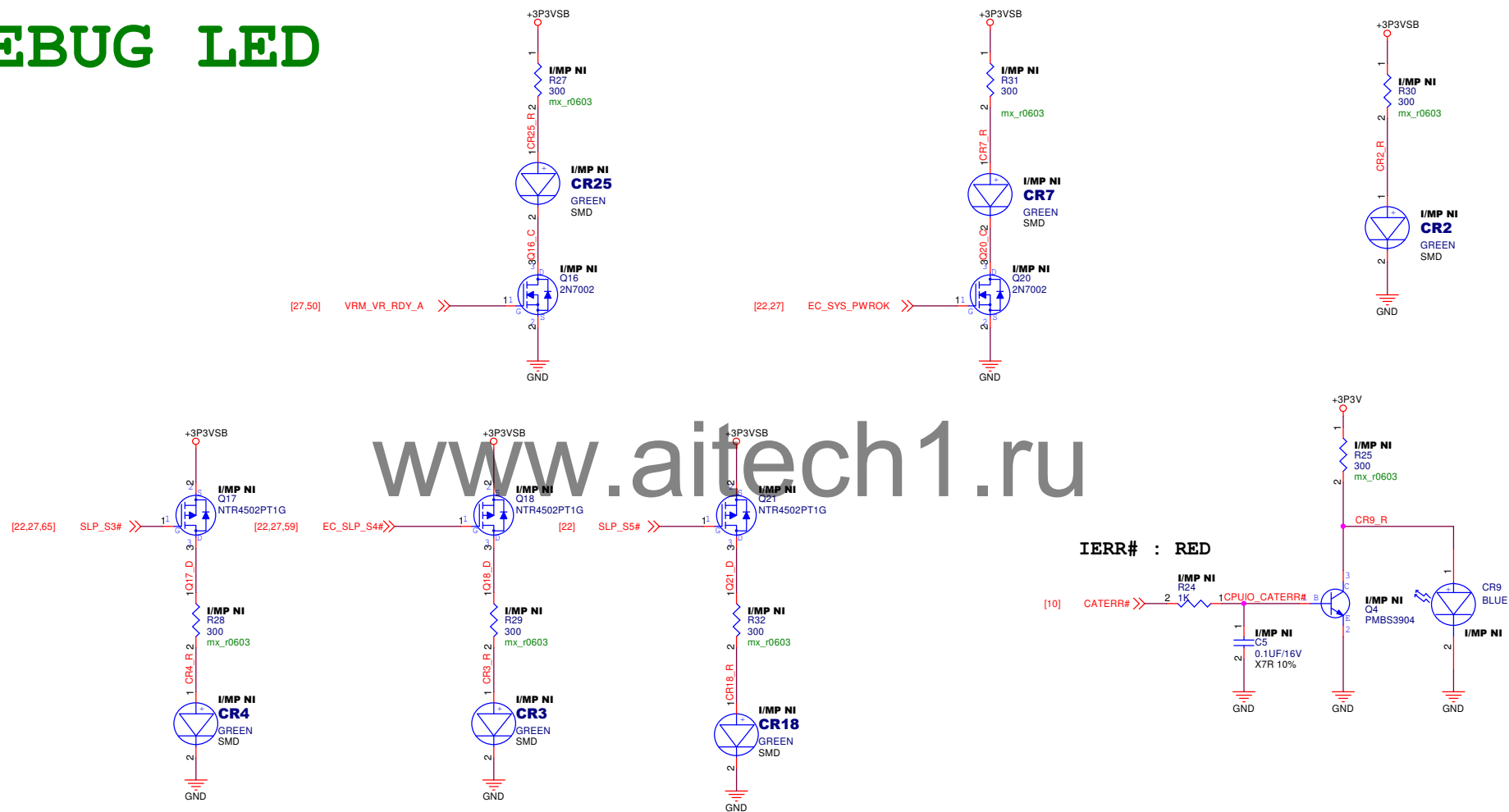
### NOTE:

PWRBTN# of PCH is internally pulled-up in PCH to 3.3 V DSW through a weak pull-up 24Kohm.

Gaming

<b>PEGATRON</b>		Title : Power Button / LED	
PEGATRON CORPORATION		Engineer: Ken_Huang	
Size A3	Project Name IPMSL-GM	Rev R1.01	
Date: Tuesday, March 15, 2016		Sheet 43 of 65	

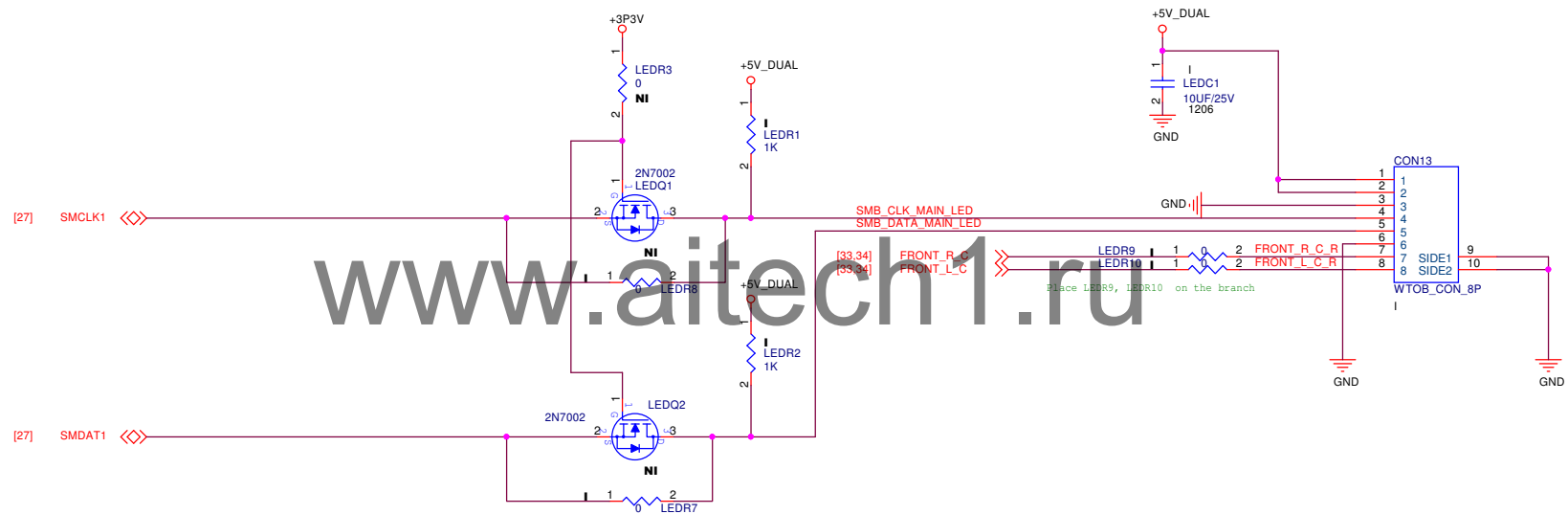
# DEBUG LED



Gaming

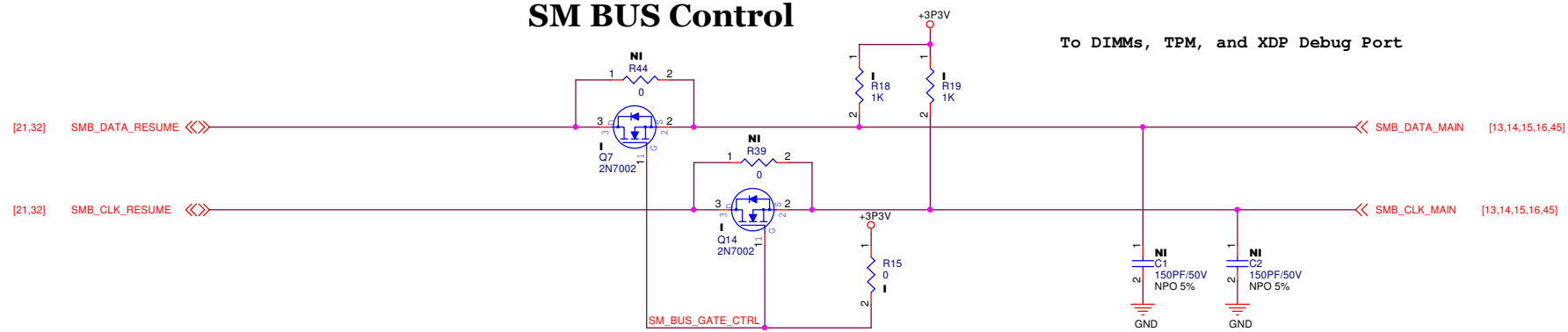


# LED\_BAR

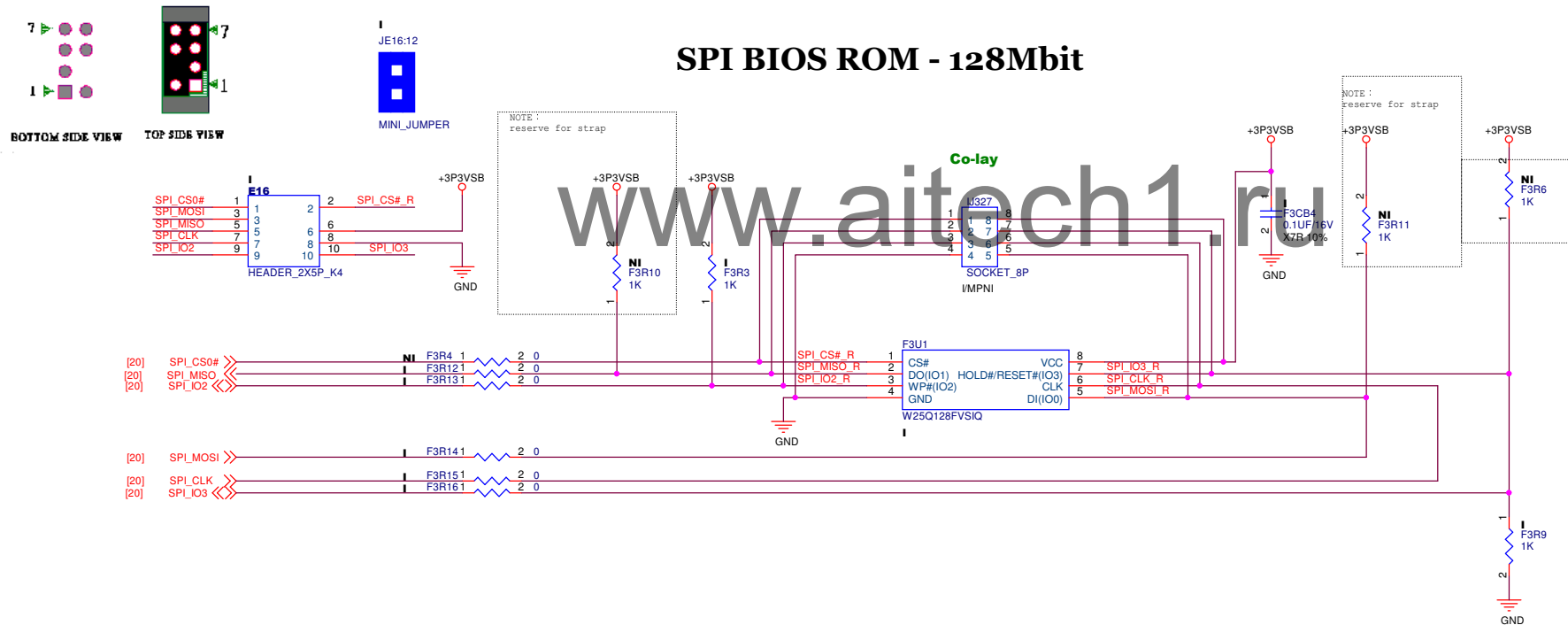


Gaming

# SM BUS Control



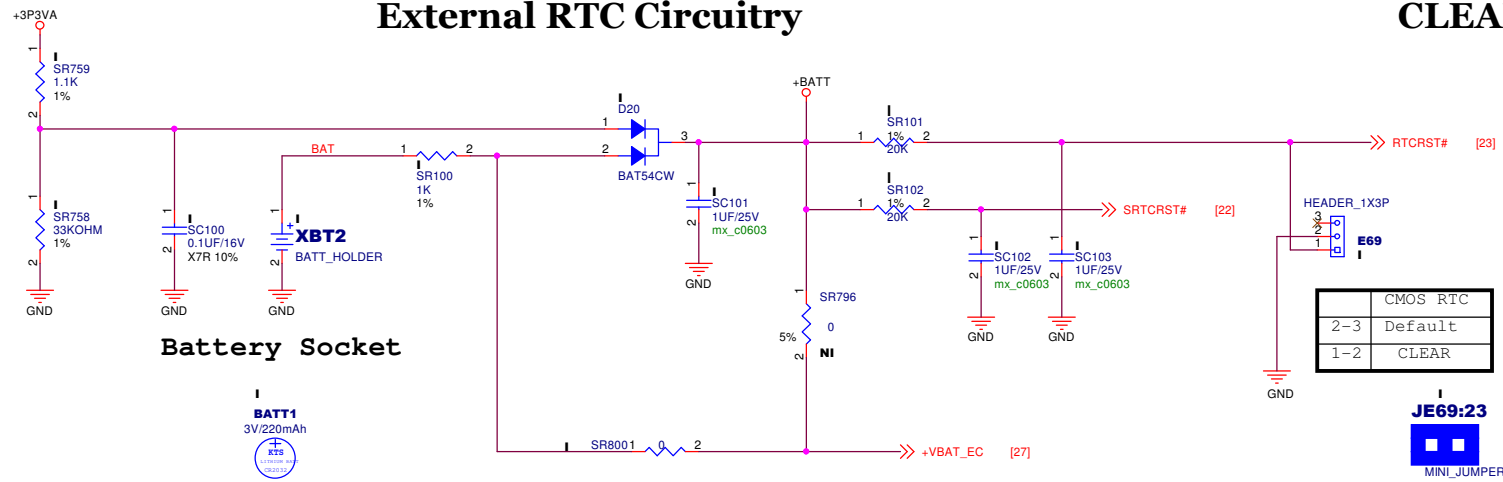
# SPI BIOS ROM - 128Mbit



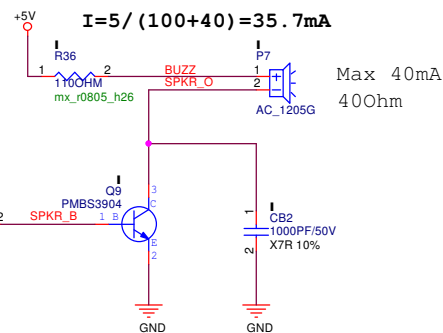
Gaming

## External RTC Circuitry

## CLEAR CMOS



## SPEAKER

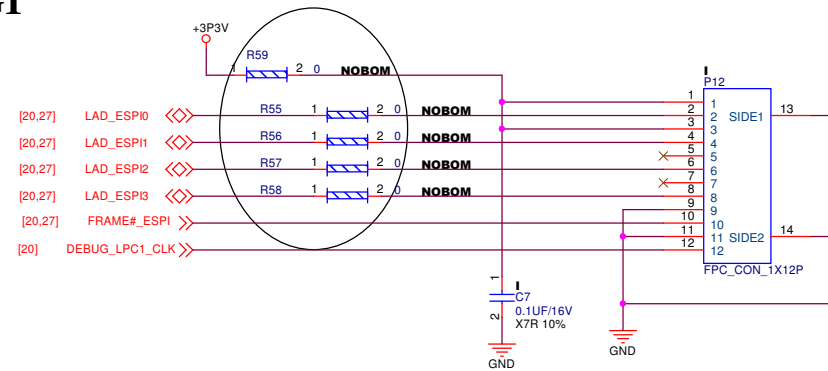


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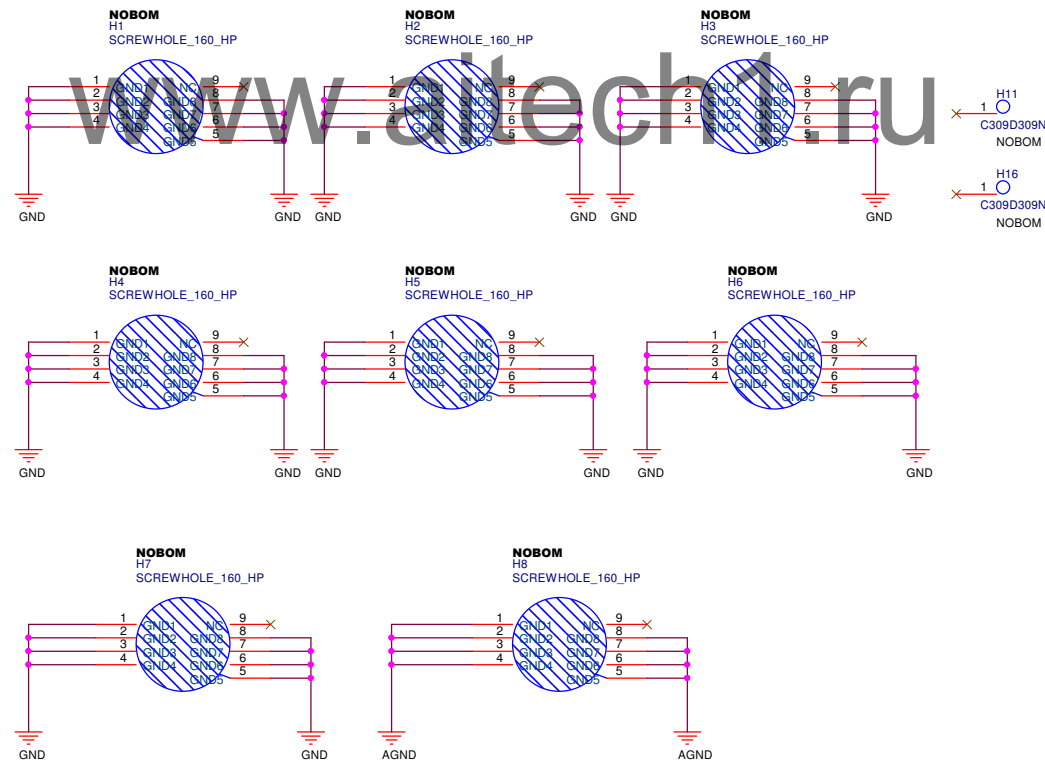
Gaming

PEGATRON		Title : RTC / CMOS	
PEGATRON CORPORATION		Engineer: Ken_Huang	
Size A3	Project Name IPMSL-GM	Rev R1.01	
Date: Tuesday, March 15, 2016		Sheet 47 of 65	

# LPC DEBUG1



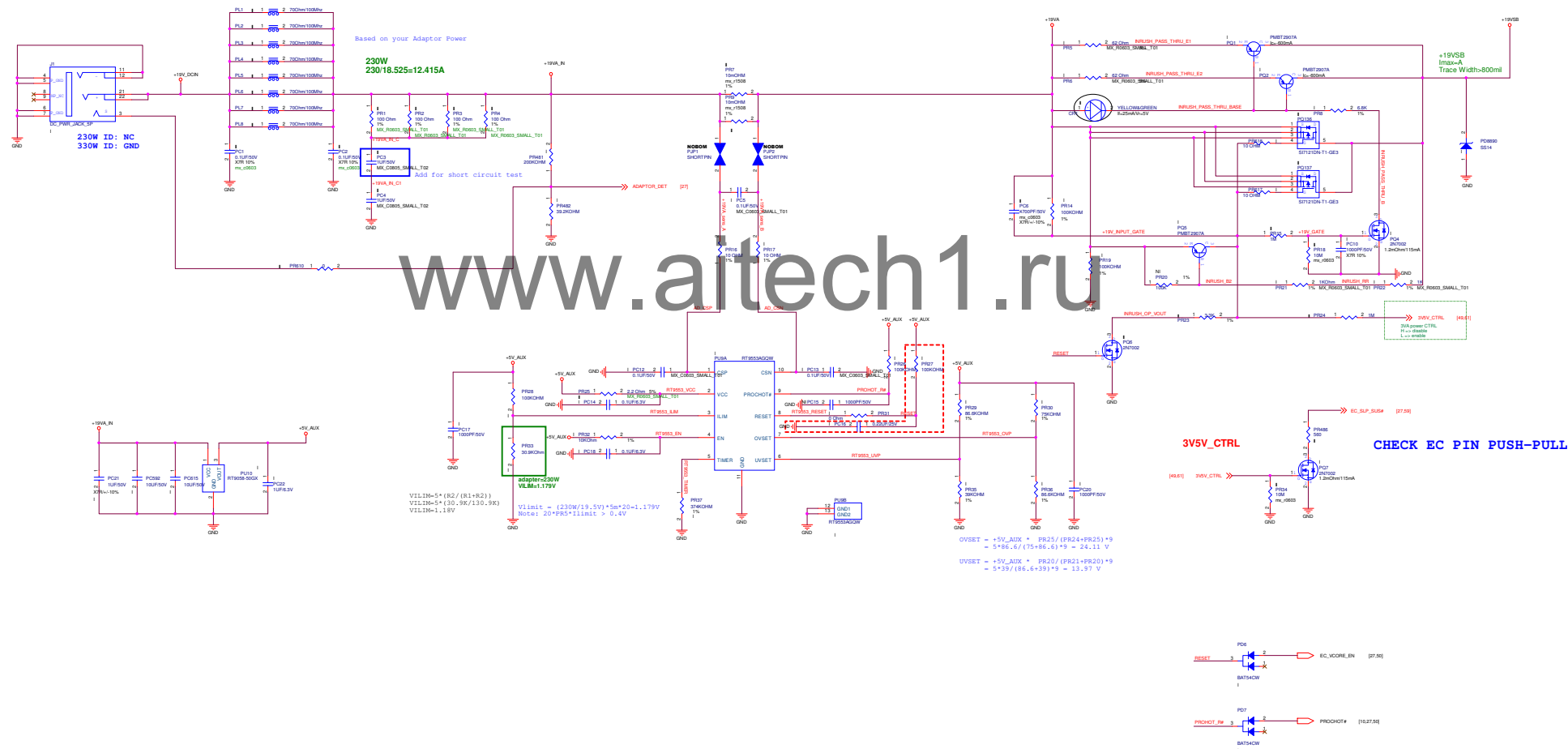
## ONLY FOR INTEL SCREW HOLE



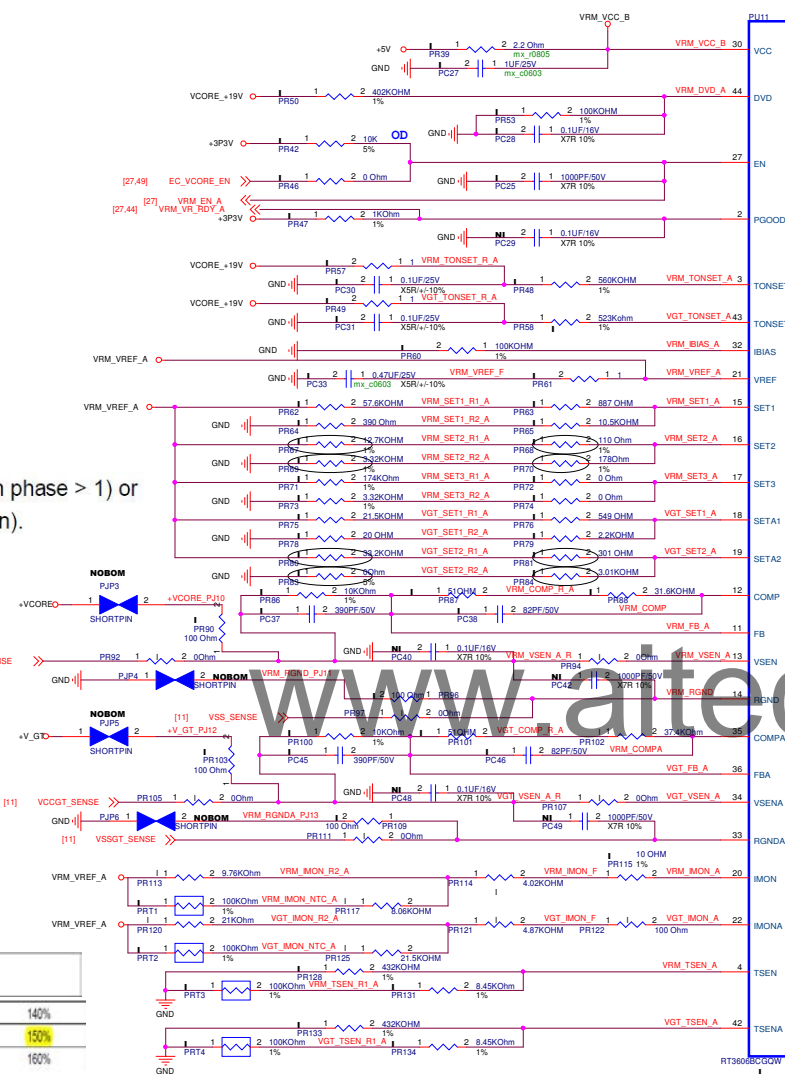
Gaming

<b>PEGATRON</b>		Title : LPC DEBUG	
PEGATRON CORPORATION		Engineer: Ken_Huang	
Size A3	Project Name IPMSL-GM		Rev R1.01
Date: Tuesday, March 15, 2016		Sheet 48 of 65	

**+19VSB**



## +VCORE



level if  $V_{IMON} - V_{REF} = 1.6V$  (for maximum phase > 1) or  $V_{IMON} - V_{REF} = 0.4$  (for 1-phase application).

$$V_{\text{IMON}} - V_{\text{REF}} = \frac{\text{DCR}}{R_{\text{CS}}} \times R_{\text{EQ}} \times (I_{\text{L1}} + I_{\text{L2}} + I_{\text{L3}})$$

$1.6 = 0.98 \text{ m ohm} / 680 \text{ ohm} * \text{REQ} * 80\text{A}$   
 $\text{REQ} = 13.87 \text{ k ohm}$   
 $\text{REQ} = 10 \text{ ohm} + \text{PR114} + (9.76 \text{ k ohm} // (100 \text{ k ohm} + 8.06 \text{ k ohm}))$   
 $\text{PR114} = 4.9 \text{ k ohm}$

$\Delta V_{SET1} = 80 \mu A \times \frac{R1 \times R2}{R1 + R2}$				
700.684	711.632	722.581	mV	<div>45.5mV</div> <div>150mV</div> <div>140%</div> <div>160%</div>
725.709	736.657	747.605	mV	
750.733	761.681	772.630	mV	

VSET1 = $\frac{R2}{R1+R2} \times 3.2V$			ICCMAX	Unit	
Min	Typical	Max	Unit		
475.464	478.592	481.720	mV	76	A
487.977	491.105	494.233	mV	78	A
500.489	503.617	506.745	mV	80	A
513.001	516.129	519.257	mV	82	A

### Vcore OCP Point Setting Check

OWNER	OCF Point	Low Limited	High Limited
Mao	120A	91.07A	40A@0.146uH
Mark	120A	91.07A	40A@0.146uH



if  $V_{IMONA} - V_{REF} = 1.6V$  (for maximum phase >1) or  
 $V_{IMONA} - V_{REF} = 0.4V$  (for 1-phase application)

$$V_{IMONA} - V_{REF} = \frac{DCR}{R_{CSA}} \times R_{EQA} \times (I_{LA1} + I_{LA2})$$

$\Delta V_{GS(T)} = 50\mu A$ R1-R2 R1+R2				DVID_Threshold		OCP = 1UCCMAX
Min	Typical	Max	Unit	DVID SR = 10mV/us	DVID SR = 20mV/us	
0.000	10.948	21.899	mV			NA
25.024	35.973	46.921	mV			110%
50.049	60.997	71.945	mV			120%
75.073	86.022	96.970	mV	13.33mV	40mV	140%
100.098	111.046	121.994	mV			160%
125.122	136.070	147.019	mV			150%
150.147	161.095	172.043	mV			160%

1.6=0.98 m ohm/680 ohm \* REQ\*46A  
REQ=24.13k ohm

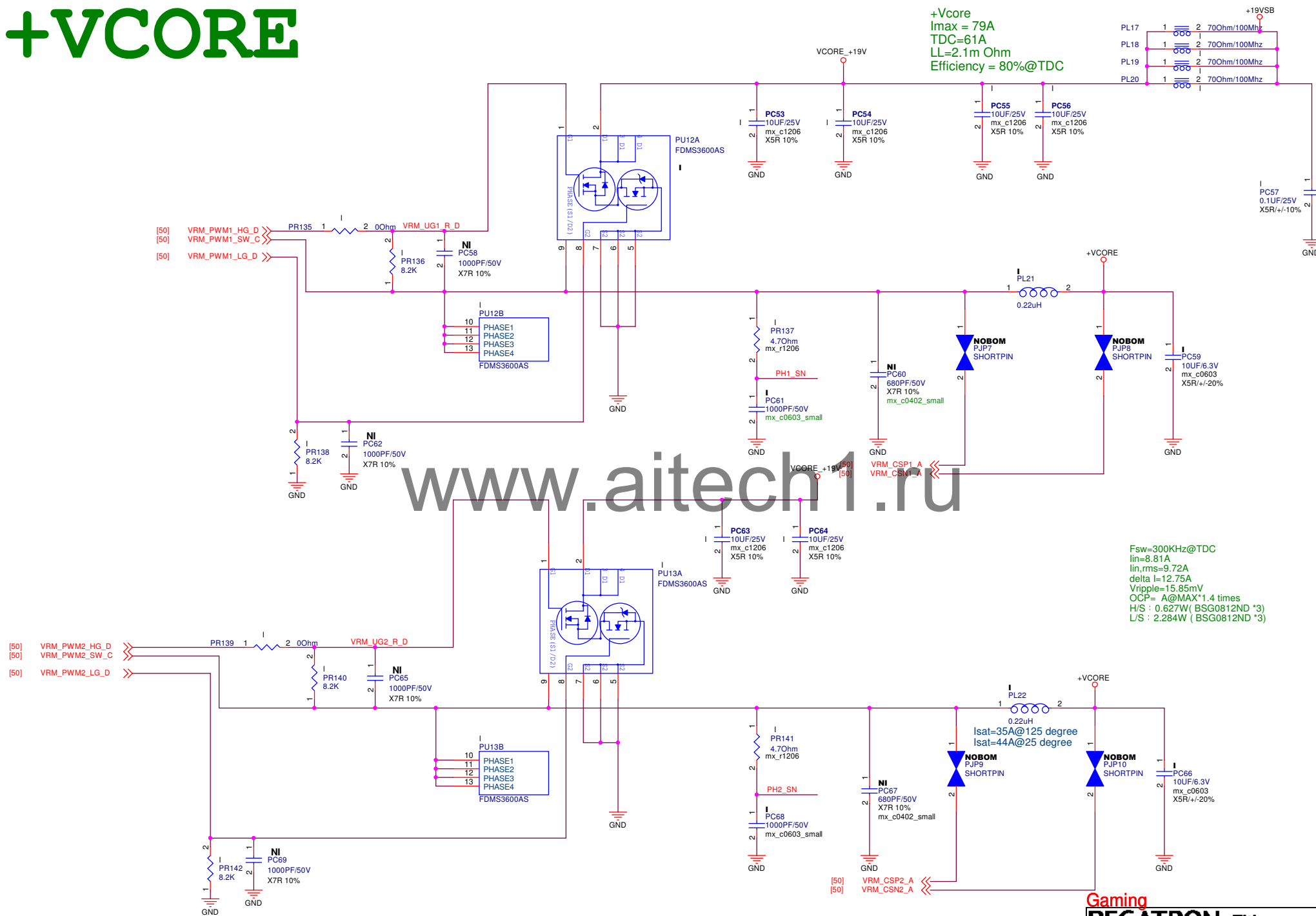
REQ= 100 ohm+ PR121+(21k ohm/((100k ohm+21.5k ohm))  
PR114= 6.12k ohm

### VGT OCP Point Setting Check

OWNER	OCF Point	Low Limited	High Limited
Mao	73.6A	54.44A	36.8A@0.14uH
Mark	73.6A	54.44A	36.8A@0.14uH

$$\begin{aligned} V_{set1} &= 80\mu A * [(22.049k * 2.2k) / (22.049k + 2.2k)] ohm = 160mV \\ V_{set1} &= 2.2k / (22.049k + 2.2k) * 3.2V = 290mV \\ I_{limit} &= 160\% * I_{CCMAX} = 1.6 * 46 = 73.6A \end{aligned}$$

# +V CORE



Gaming

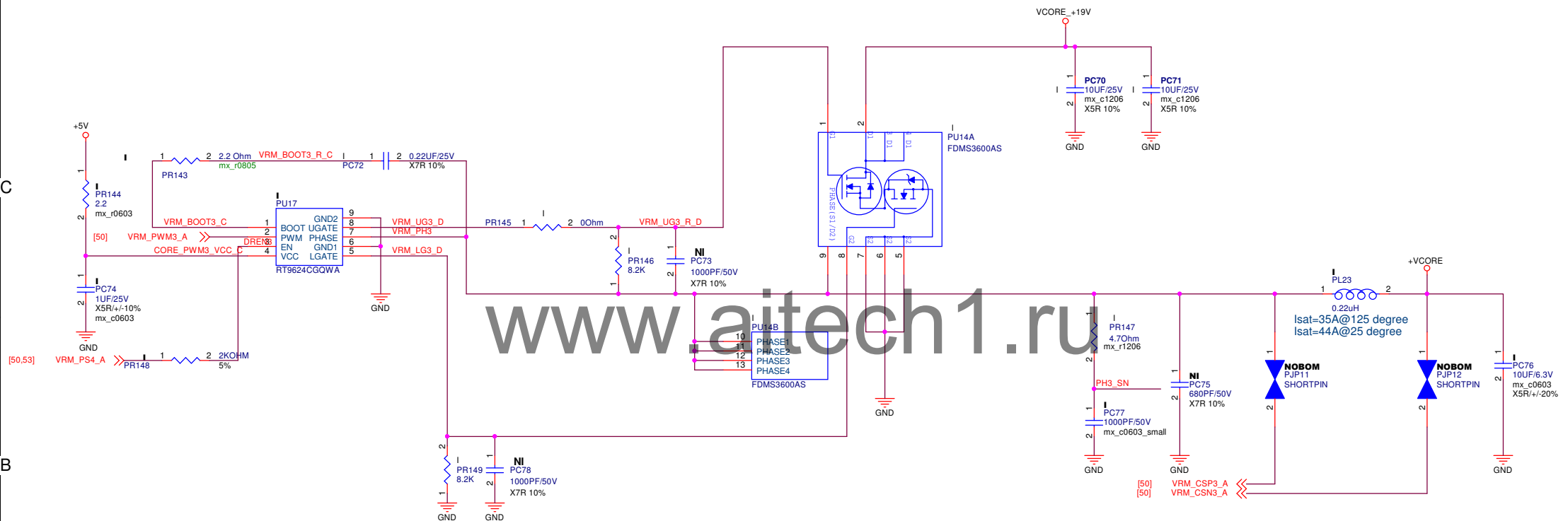
**PEGATRON** Title : **V CORE DRIVER 1**

PEGATRON CORPORATION Engineer: **Ken\_Huang**

Size	Project Name	Rev
A3	<b>IPMSL-GM</b>	R1.01

Date: Tuesday, March 15, 2016 Sheet 51 of 65

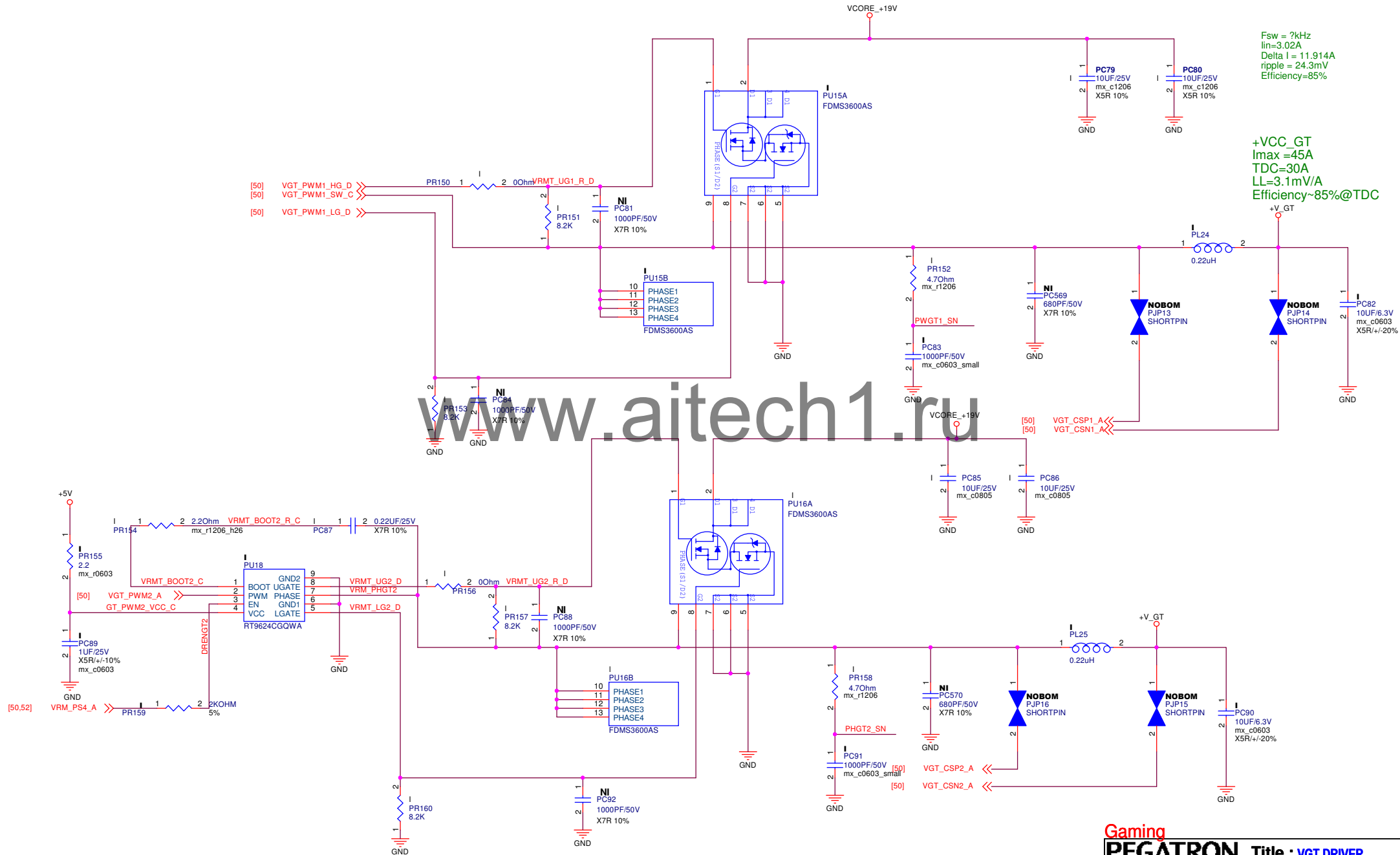
# +VCORE



VCORE Heatsink ??



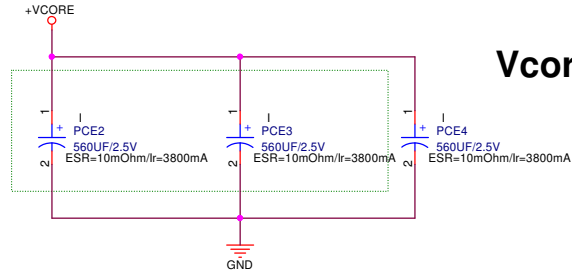
# +V\_GT



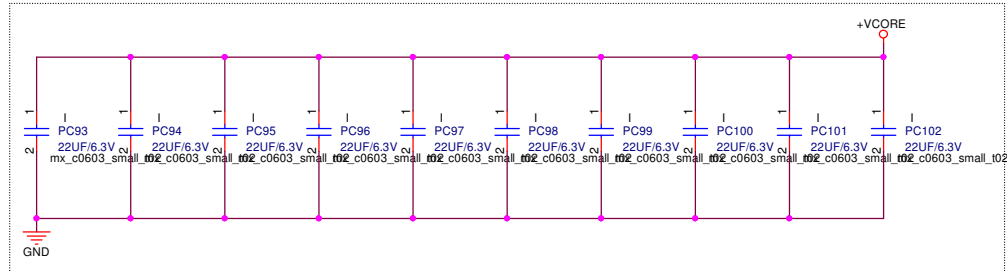
Fsw = 7kHz  
Iin=3.02A  
Delta I = 11.914A  
ripple = 24.3mV  
Efficiency=85%

+VCC\_GT  
Imax =45A  
TDC=30A  
LL=3.1mV/A  
Efficiency~85%@TDC

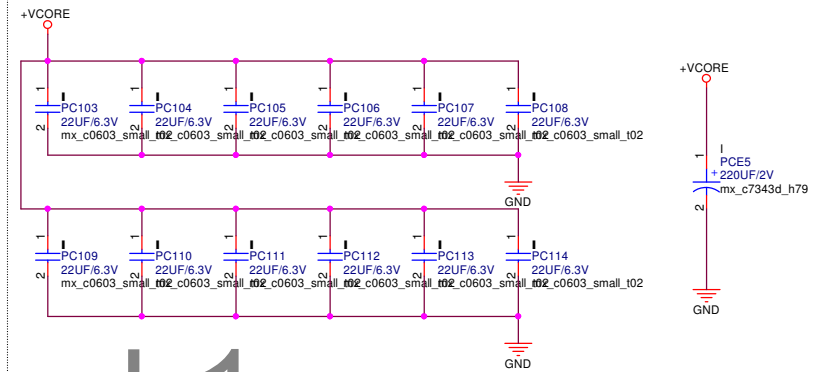
## Vcore Output CAP



On Socket Top Side



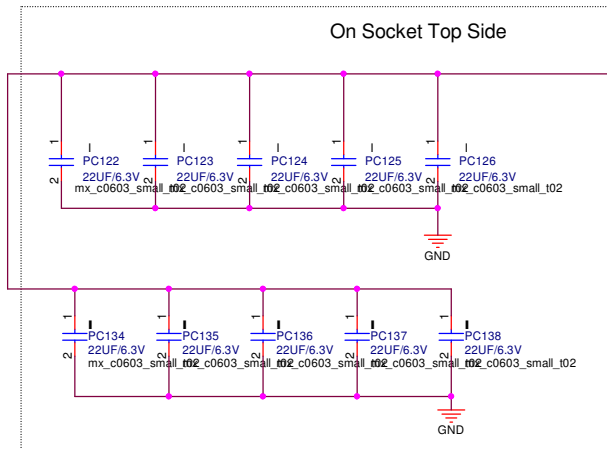
On Socket Bottom Side



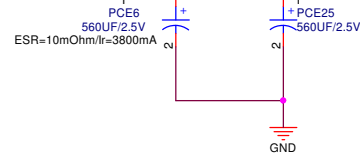
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## V\_GT Output CAP

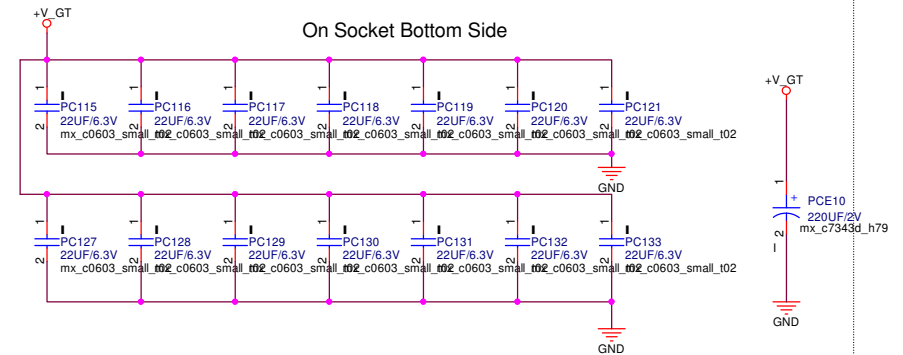
On Socket Top Side



Change part to 1B09-00PQZ00



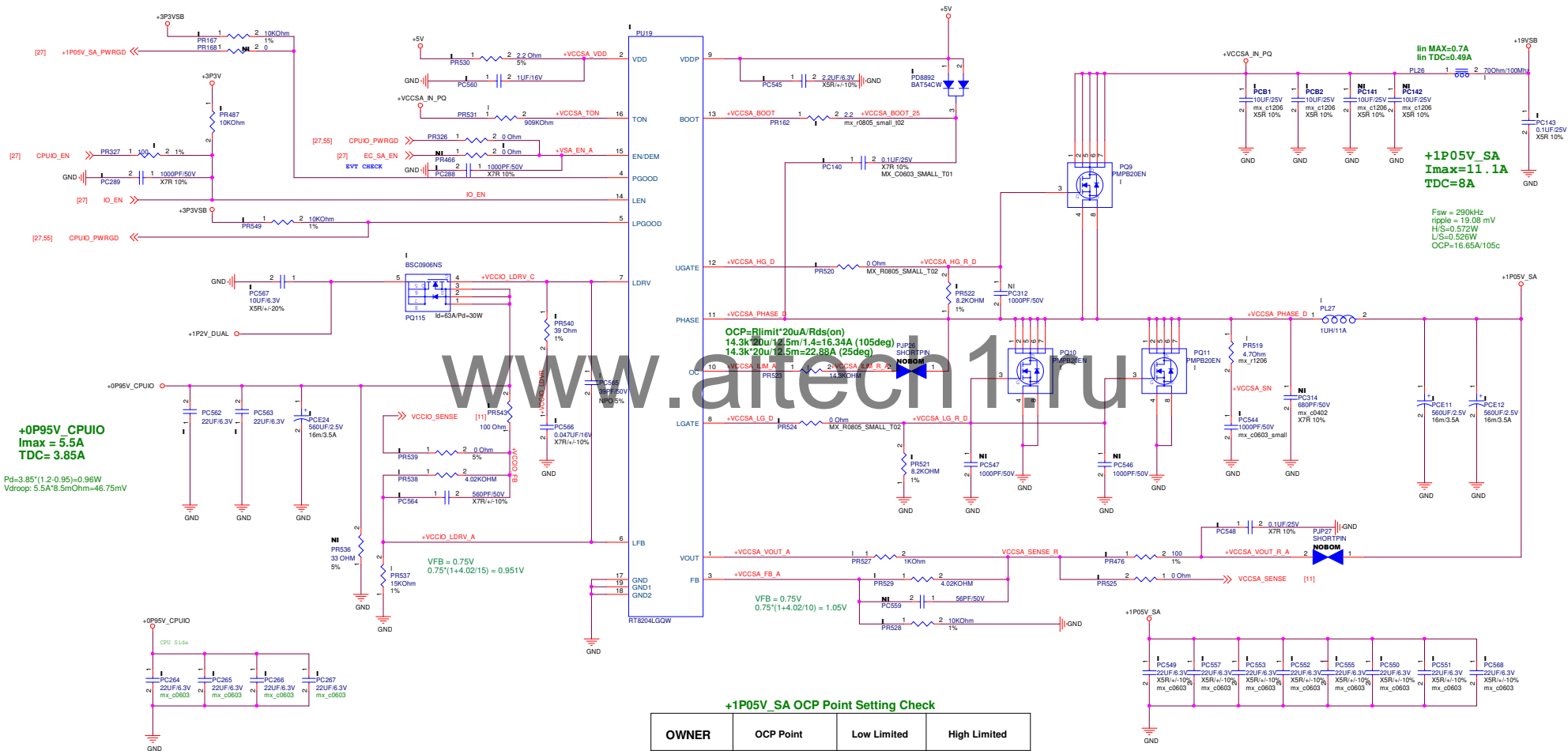
On Socket Bottom Side



Gaming

## +0P95V\_CPUIO

+1P05V\_SA

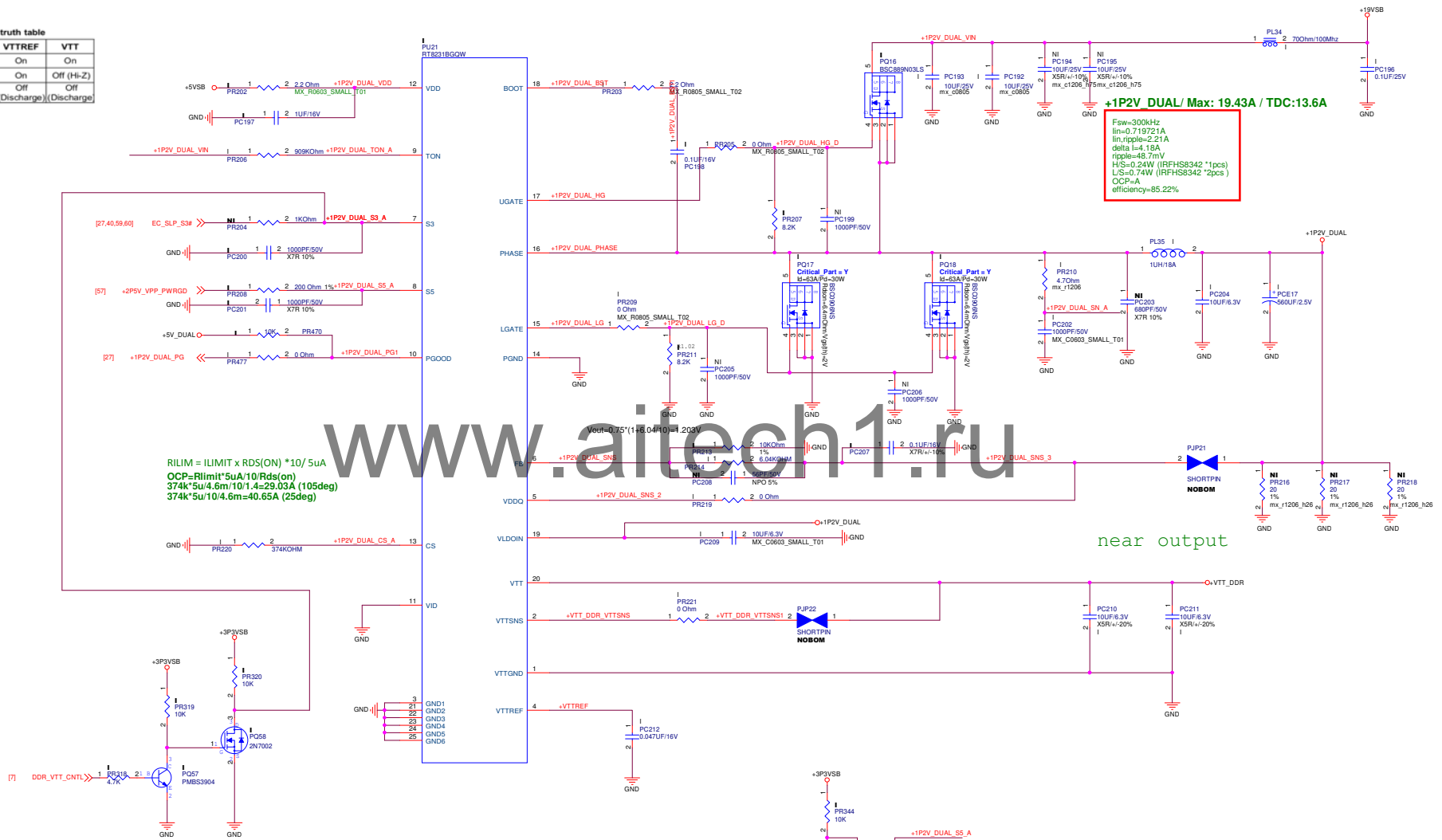


OWNER	OCF Point	Low Limited	High Limited
Mao	16.34A@105deg 22.88@25deg	11.1A	22.88A@0.8uH
Mark	16.34A@105deg 22.88@25deg	11.1A	22.88A@0.8uH

# +1P2V\_DUAL

Table 2. S3 and S5 truth table

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)



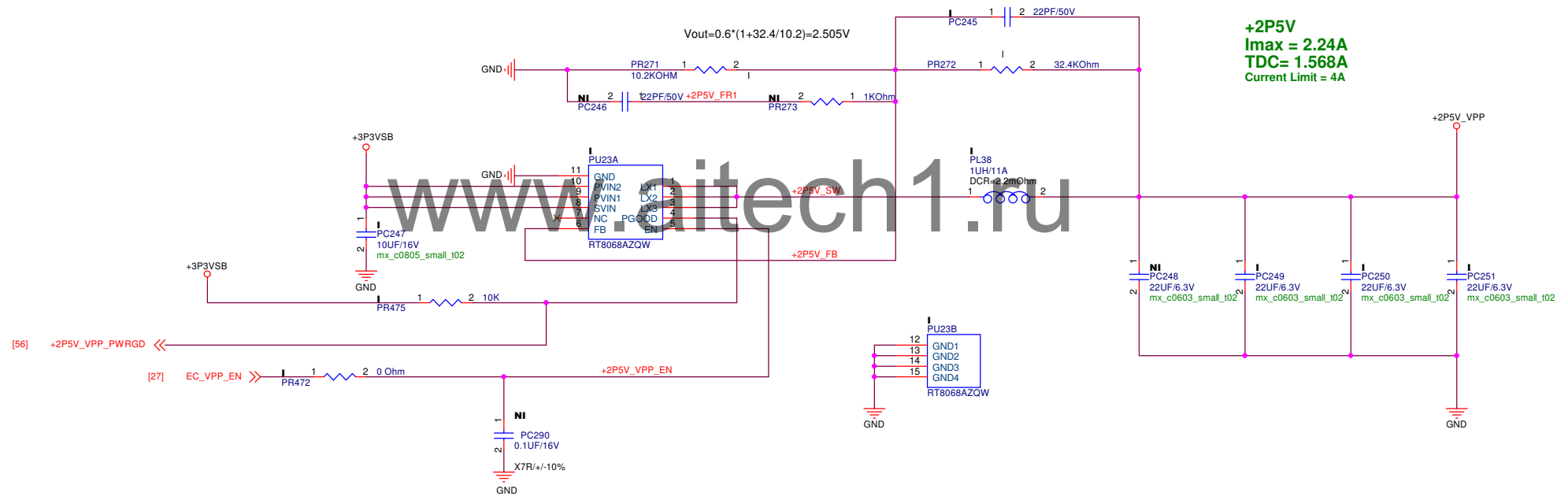
RILIM = ILIMIT x RDS(ON) \* 10 / 5uA  
 OCP=RIlimit\*5uA/10/Rds(on)  
 374k\*5u/4.6m/10/1.4=29.03A (105deg)  
 374k\*5u/10/4.6m=40.65A (25deg)

+1P2V\_DUAL/ Max: 19.43A / TDC:13.6A  
 Fsw=300kHz  
 Iin=0.719721A  
 Iin\_ripple=2.21A  
 delta I=4.18A  
 ripple=48.7mV  
 H/S=0.24W (IRFHS8342 \*1pcs)  
 L/S=0.74W (IRFHS8342 \*2pcs)  
 OCP=A  
 efficiency=85.22%

+1P2V\_Dual OCP Point Setting Check

OWNER	OCP Point	Low Limited	High Limited
Mao	29.03A@105deg 40.65@25deg	19.43A	40.65A@0.8uH
Mark	29.03A@105deg 40.65@25deg	19.43A	40.65A@0.8uH

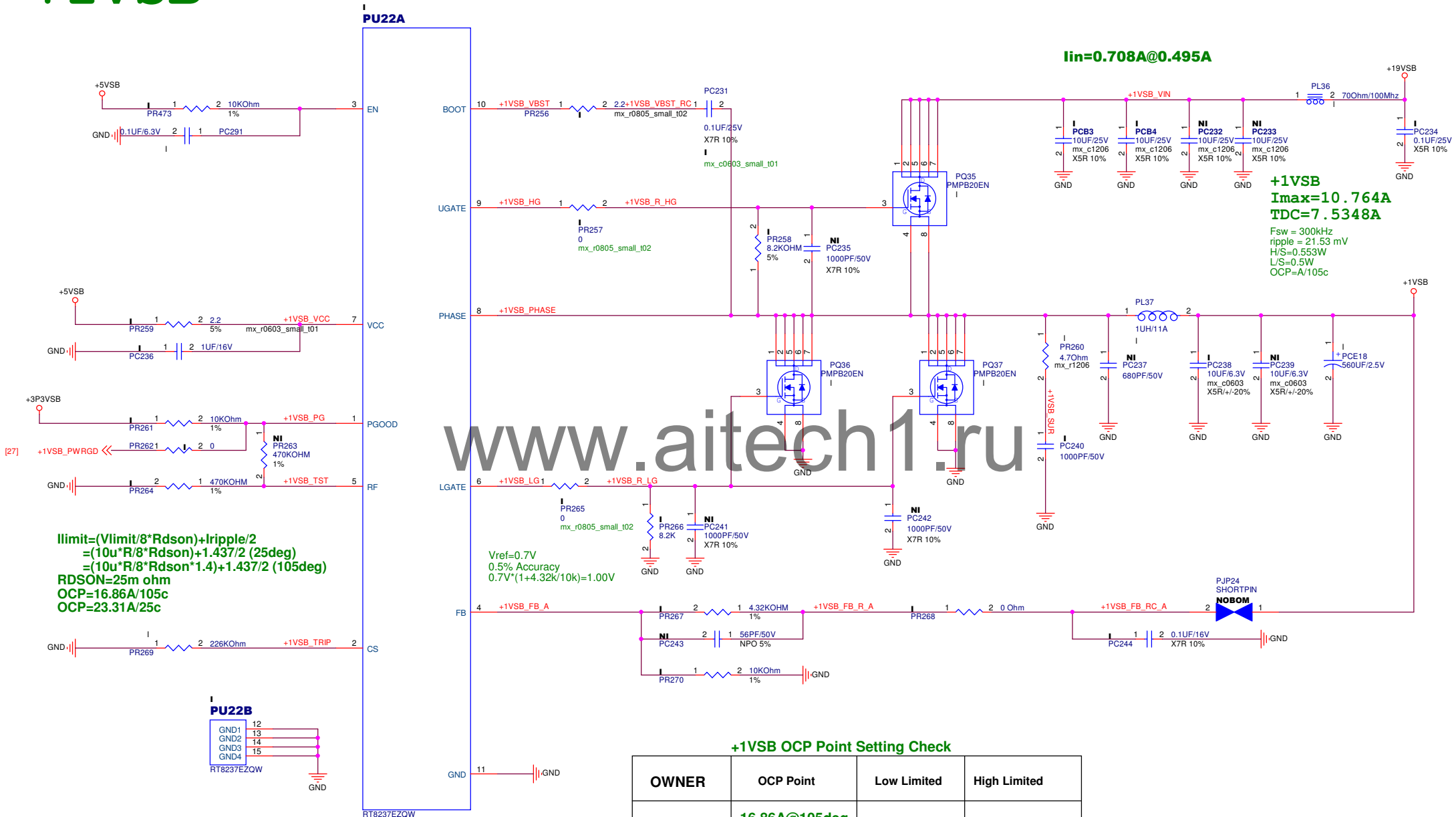
**+2P5V\_VPP**



## Gaming

<b>PEGATRON</b>		Title : <b>+2P5V_VPP</b>	
PEGATRON CORPORATION		Engineer: <b>Ken_Huang</b>	
Size <b>A3</b>	Project Name <b>IPMSL-GM</b>	Rev <b>RI.01</b>	
Date: <b>Tuesday, March 15, 2016</b>	Sheet	<b>57</b>	of <b>65</b>

# +1VSB



$I_{limit} = (V_{limit}/8 \cdot R_{dson}) + I_{ripple}/2$   
 $= (10\mu \cdot R/8 \cdot R_{dson}) + 1.437/2 \text{ (25deg)}$   
 $= (10\mu \cdot R/8 \cdot R_{dson} \cdot 1.4) + 1.437/2 \text{ (105deg)}$   
 $R_{DSON} = 25m \text{ ohm}$   
 $OCP = 16.86A/105c$   
 $OCP = 23.31A/25c$

$V_{ref} = 0.7V$   
 $0.5\% \text{ Accuracy}$   
 $0.7V \cdot (1 + 4.32k/10k) = 1.00V$

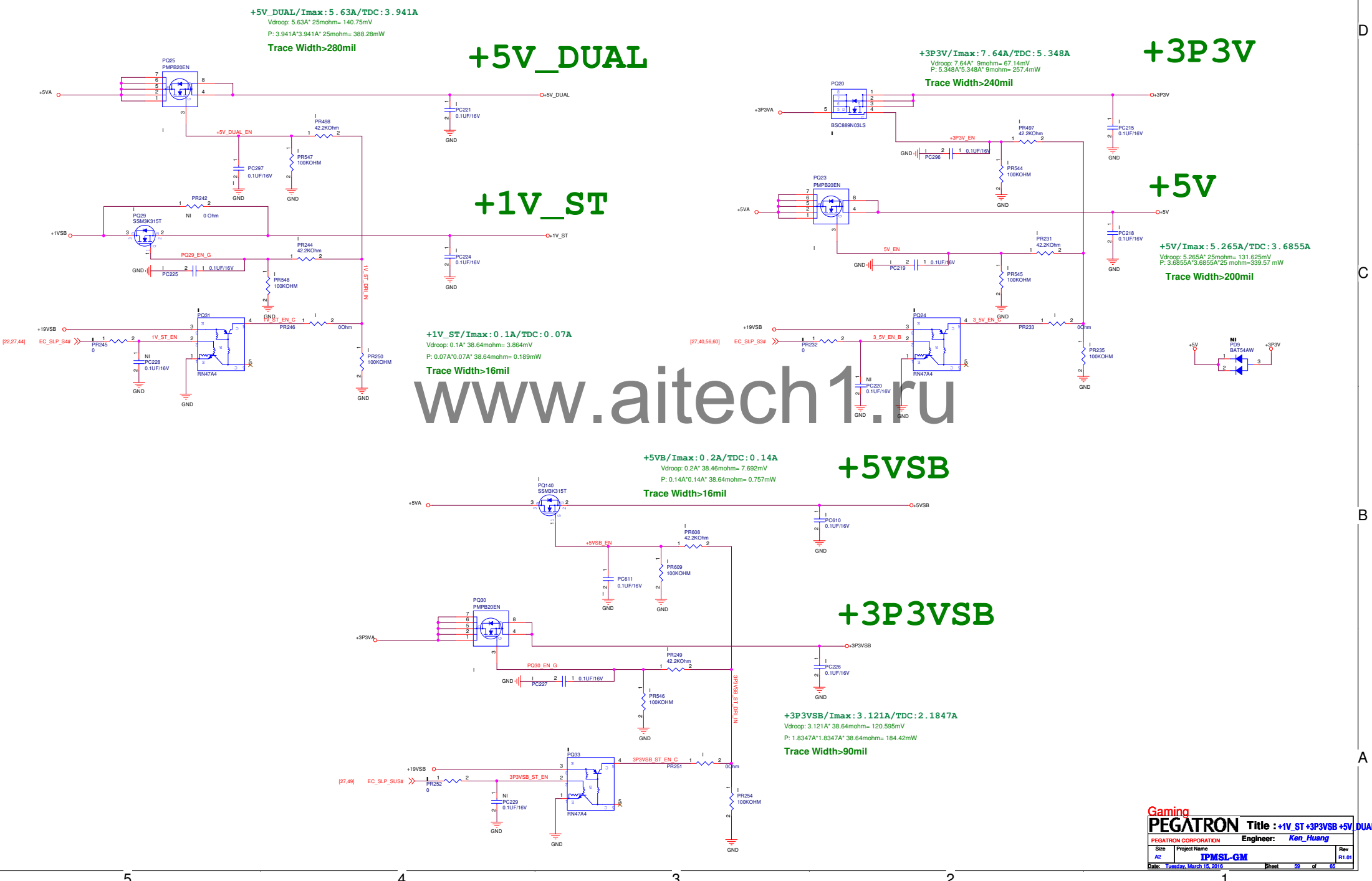
## +1VSB OCP Point Setting Check

OWNER	OCP Point	Low Limited	High Limited
Mao	16.86A@105deg 23.31@25deg	10.764A	23.31A@0.8uH
Mark	16.86A@105deg 23.31@25deg	10.764A	23.31A@0.8uH

**Iin=0.708A@0.495A**

**+1VSB**  
 $I_{max} = 10.764A$   
 $TDC = 7.5348A$

$F_{sw} = 300kHz$   
 $ripple = 21.53 \text{ mV}$   
 $H/S = 0.553W$   
 $L/S = 0.5W$   
 $OCP = A/105c$



**+5V\_DUAL/Imax: 5.63A/TDC: 3.941A**  
Vdroop: 5.63A\*25mohm= 140.75mV  
P: 3.941A\*3.941A\*25mohm= 388.28mW  
Trace Width>280mil

**+5V\_DUAL**

**+3P3V/Imax: 7.64A/TDC: 5.348A**  
Vdroop: 7.64A\* 9mohm= 67.14mV  
P: 5.348A\*5.348A\* 9mohm= 257.4mW  
Trace Width>240mil

**+3P3V**

**+1V\_ST**

**+1V\_ST/Imax: 0.1A/TDC: 0.07A**  
Vdroop: 0.1A\* 38.64mohm= 3.864mV  
P: 0.07A\*0.07A\* 38.64mohm= 0.189mW  
Trace Width>16mil

**+5V**

**+5V/Imax: 5.265A/TDC: 3.6855A**  
Vdroop: 5.265A\*25mohm= 131.625mV  
P: 3.6855A\*3.6855A\*25mohm= 339.57mW  
Trace Width>200mil

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**+5VSB/Imax: 0.2A/TDC: 0.14A**  
Vdroop: 0.2A\* 38.64mohm= 7.692mV  
P: 0.14A\*0.14A\* 38.64mohm= 0.757mW  
Trace Width>16mil

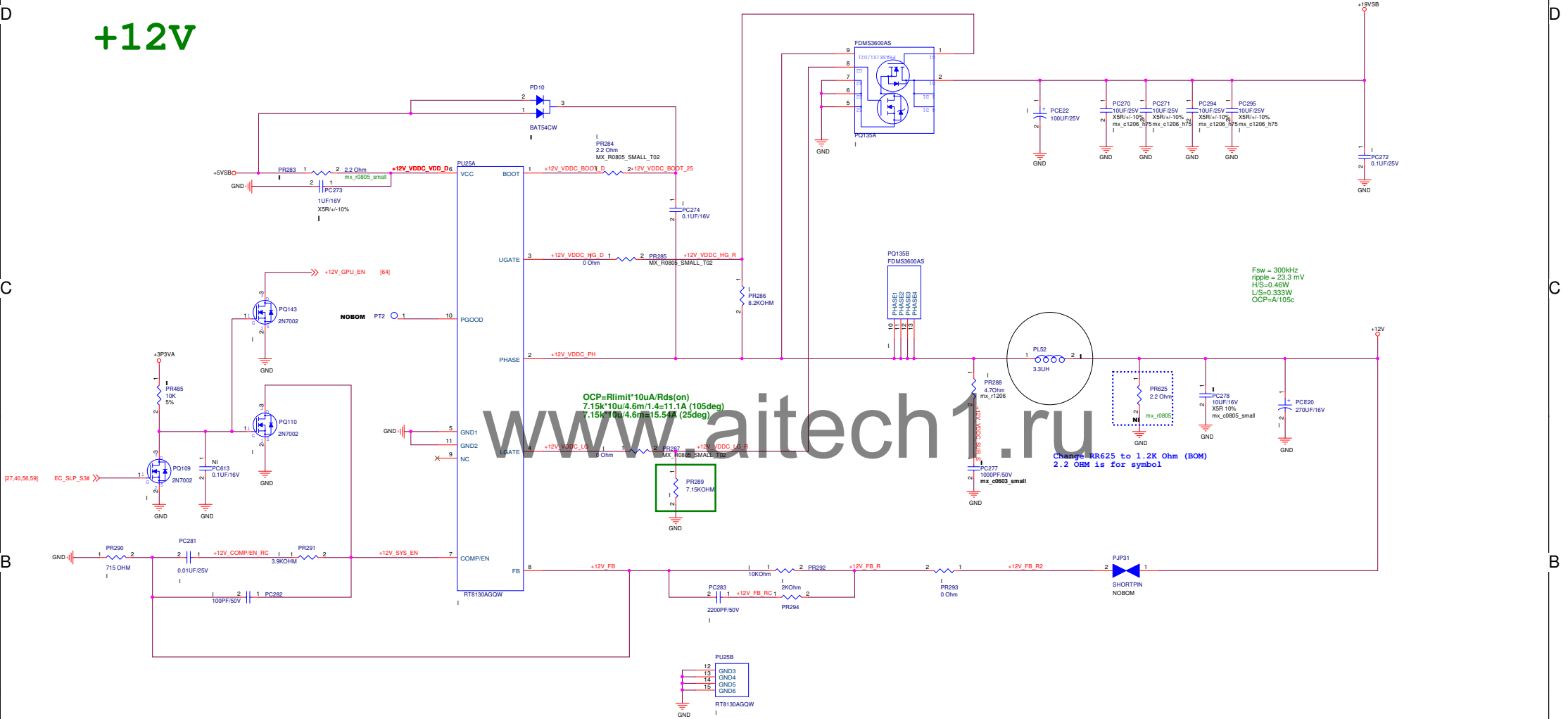
**+5VSB**

**+3P3VSB**

**+3P3VSB/Imax: 3.121A/TDC: 2.1847A**  
Vdroop: 3.121A\* 38.64mohm= 120.595mV  
P: 1.8347A\*1.8347A\* 38.64mohm= 184.42mW  
Trace Width>90mil

+12V

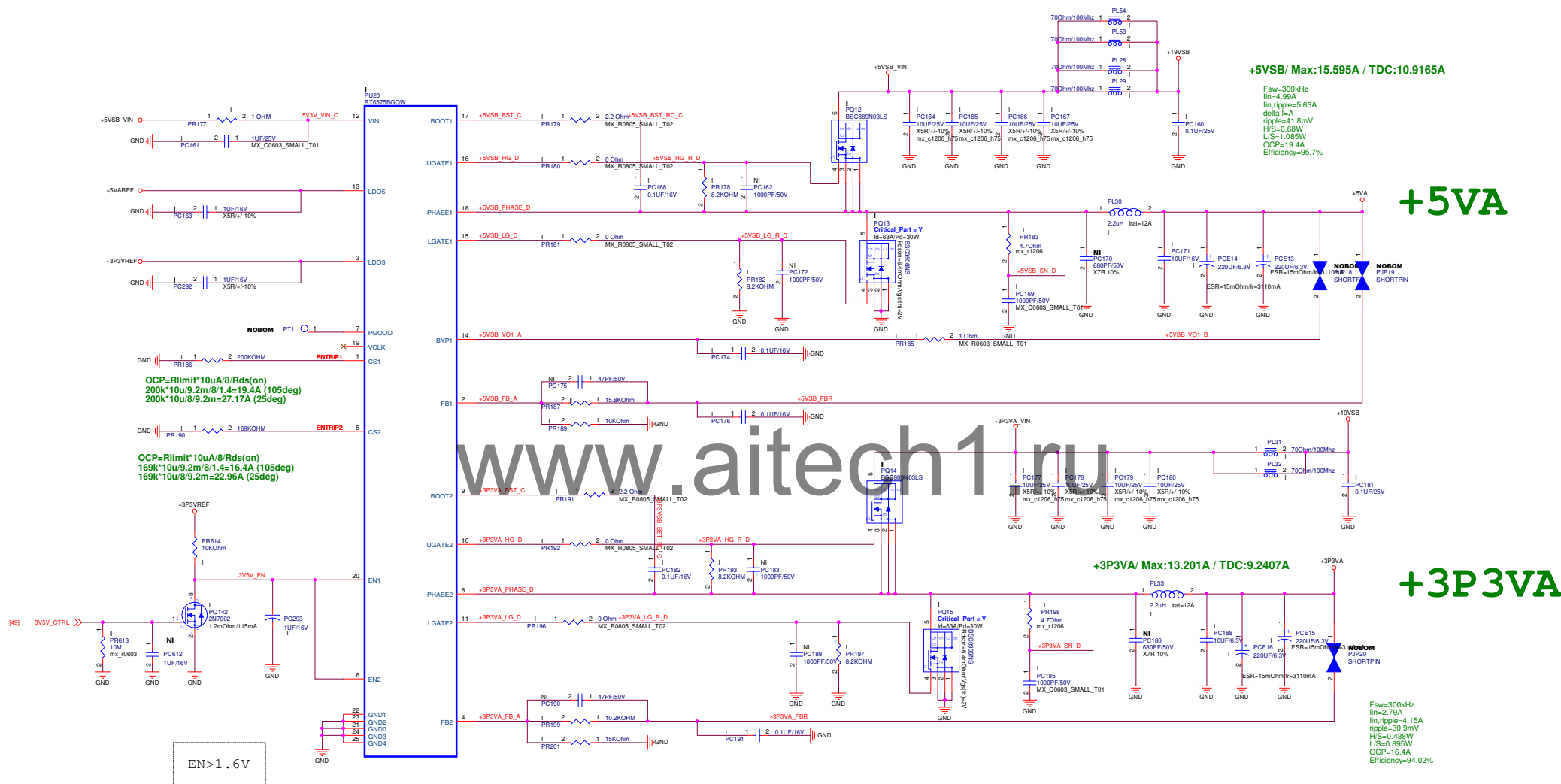
+12V  
Imax = 8.7A  
TDC = 6.09A



+12V OCP Point Setting Check

OWNER	OCP Point	Low Limited	High Limited
Mao	11.1A@105deg 15.54@25deg	8.7A	15.54A@2.64uH
Mark	11.1A@105deg 15.54@25deg	8.7A	15.54A@2.64uH





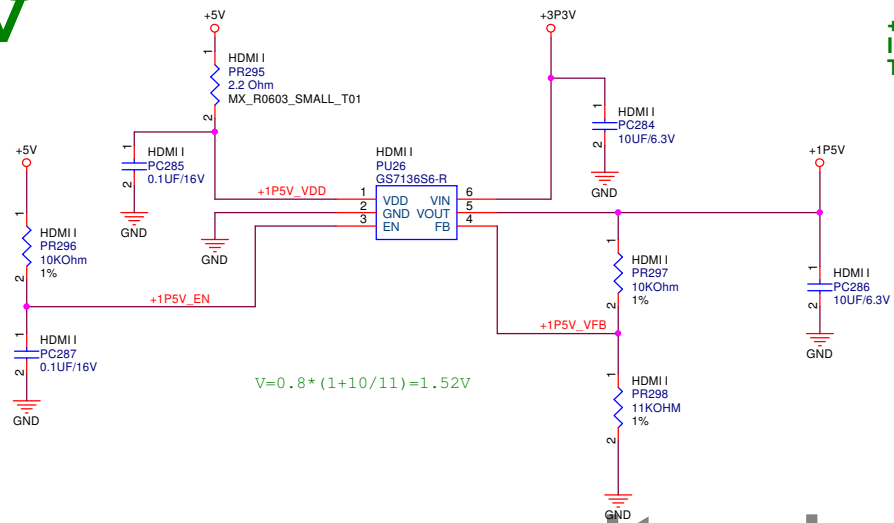
**+5VSB OCP Point Setting Check**

OWNER	OCP Point	I <sub>max</sub>	High Limited
Mao	19.4A@105deg 27.17@25deg	15.595A	1.7uH@27.17A
Mark	19.4A@105deg 27.17@25deg	15.595A	1.7uH@27.17A

**+3P3VA OCP Point Setting Check**

OWNER	OCP Point	I <sub>max</sub>	High Limited
Mao	16.4A@105deg 22.96@25deg	13.201A	1.98uH@22.96A
Mark	16.4A@105deg 22.96@25deg	13.201A	1.98uH@22.96A

+1P5V

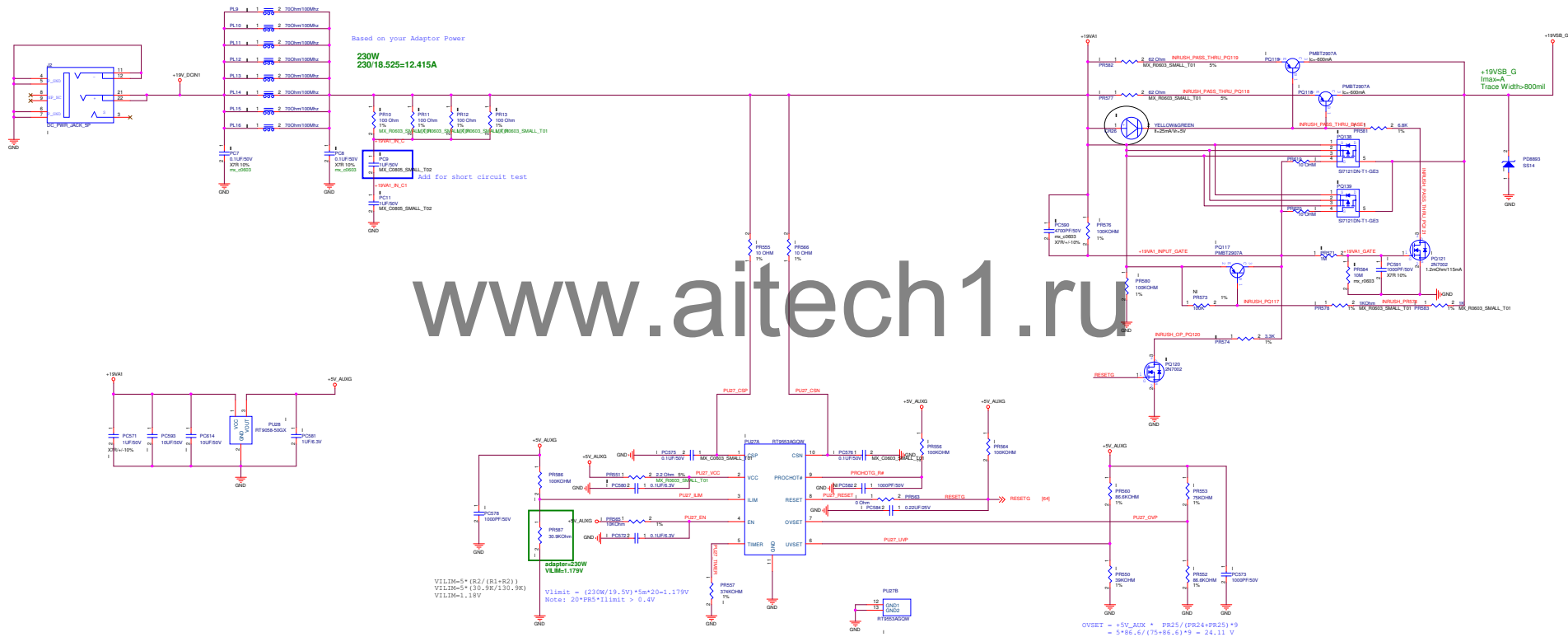


+1P5V  
I<sub>max</sub> = 0.2A  
TDC= 0.14A

$P_d = (3.3 - 1.5) \times 0.2 = 0.36W$   
 $V_{droop} = 0.2A \times 9m = 1.8mV$   
 $Eff = 45\%$   
 $OCP = 0.7A$

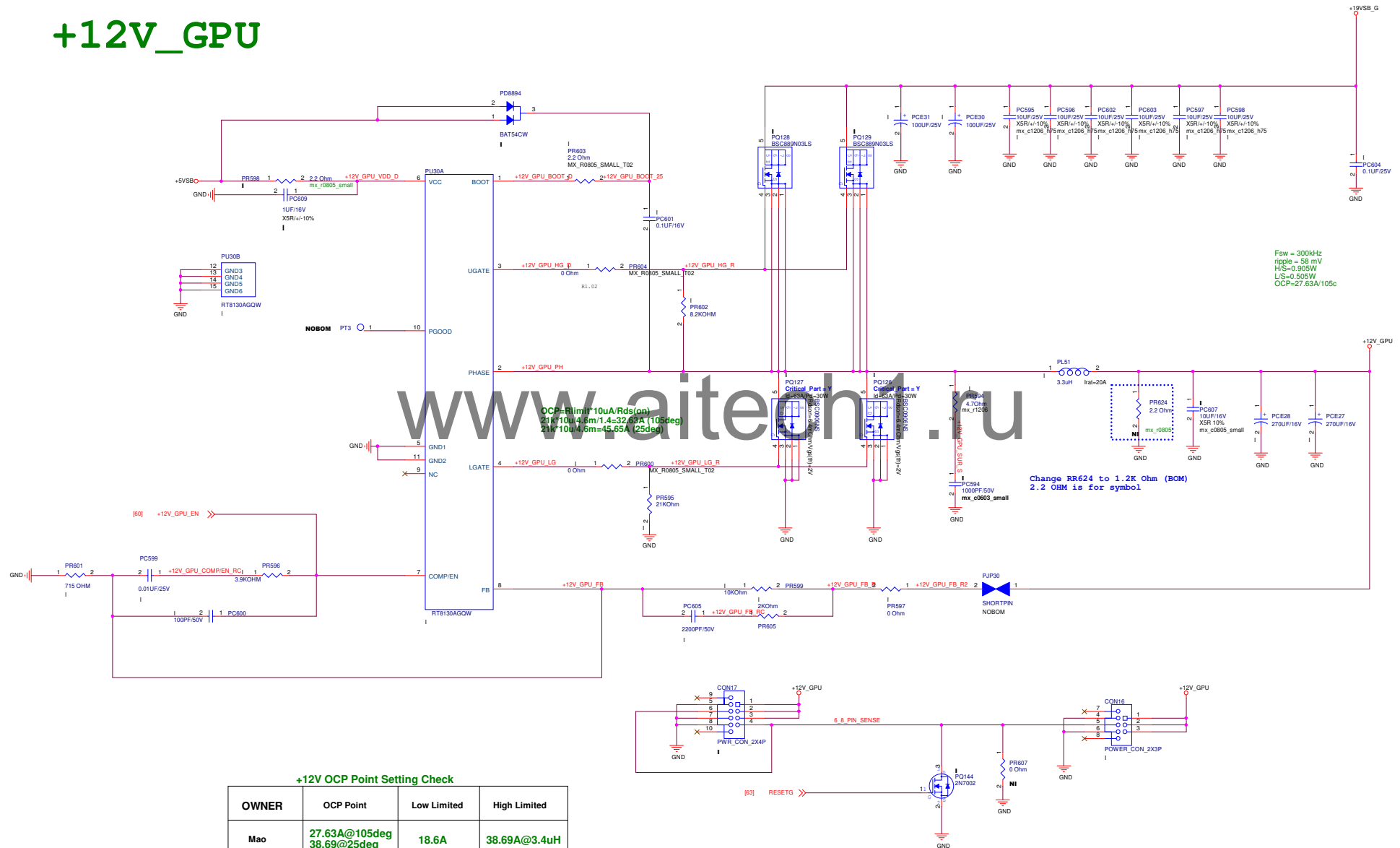
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# +19VSB\_G



# +12V\_GPU

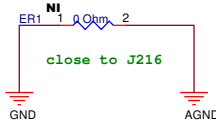
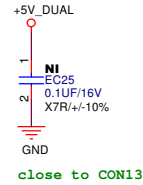
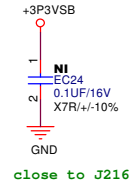
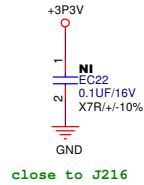
+12V\_GPU  
I<sub>max</sub> = 18.6A  
TDC = 13.02A



+12V OCP Point Setting Check

OWNER	OCP Point	Low Limited	High Limited
Mao	27.63A@105deg 38.69@25deg	18.6A	38.69A@3.4uH
Mark	27.63A@105deg 38.69@25deg	18.6A	38.69A@3.4uH

EMI CAP



## POWER Discharge

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